OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

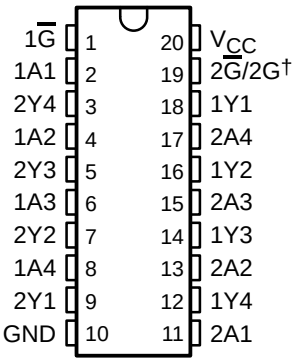
SDLS144B – APRIL 1985 – REVISED FEBRUARY 2002

- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **PNP Inputs Reduce DC Loading**
- **Hysteresis at Inputs Improves Noise Margins**

description

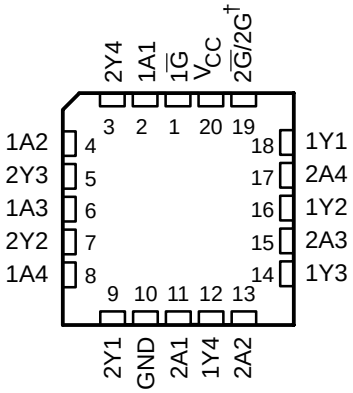
These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The designer has a choice of selected combinations of inverting and noninverting outputs, symmetrical, active-low output-control ($\overline{G}$) inputs, and complementary output-control (G and $\overline{G}$) inputs. These devices feature high fan-out, improved fan-in, and 400-mV noise margin. The SN74LS' and SN74S' devices can be used to drive terminated lines down to 133 Ω.

SN54LS', SN54S' . . . J OR W PACKAGE
SN74LS240, SN74LS244 . . . DB, DW, N, OR NS PACKAGE
SN74LS241 . . . DW, N, OR NS PACKAGE
SN74S' . . . DW OR N PACKAGE
(TOP VIEW)



† 2G for 'LS241 and 'S241 or $2\overline{G}$ for all other drivers.

SN54LS', SN54S' . . . FK PACKAGE
(TOP VIEW)



† 2G for 'LS241 and 'S241 or $2\overline{G}$ for all other drivers.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube	SN74LS240N	SN74LS240N
			SN74LS241N	SN74LS241N
			SN74LS244N	SN74LS244N
			SN74S240N	SN74S240N
			SN74S241N	SN74S241N
			SN74S244N	SN74S244N
	SOIC – DW	Tube	SN74LS240DW	LS240
		Tape and reel	SN74LS240DWR	
		Tube	SN74LS241DW	LS241
		Tape and reel	SN74LS241DWR	
		Tube	SN74LS244DW	LS244
		Tape and reel	SN74LS244DWR	
		Tube	SN74S240DW	S240
		Tape and reel	SN74S240DWR	
		Tube	SN74S241DW	S241
		Tape and reel	SN74S241DWR	
		Tube	SN74S244DW	S244
		Tape and reel	SN74S244DWR	
	SOP – NS	Tube	SN74LS240NSR	74LS240
			SN74LS241NSR	74LS241
			SN74LS244NSR	74LS244
	SSOP – DB	Tape and reel	SN74LS240DBR	LS240
			SN74LS244DBR	LS244

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

ORDERING INFORMATION (CONTINUED)

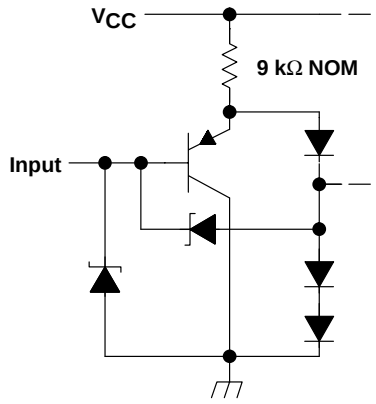
T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	CDIP – J	Tube	SN54LS240J	SN54LS240J
			SNJ54LS240J	SNJ54LS240J
			SN54LS241J	SN54LS241J
			SNJ54LS241J	SNJ54LS241J
			SN54LS244J	SN54LS244J
			SNJ54LS244J	SNJ54LS244J
			SN54S240J	SN54S240J
			SNJ54S240J	SNJ54S240J
			SN54S241J	SN54S241J
			SNJ54S241J	SNJ54S241J
			SN54S244J	SN54S244J
			SNJ54S244J	SNJ54S244J
	CFP – W	Tube	SNJ54LS240W	SNJ54LS240W
			SNJ54LS241W	SNJ54LS241W
			SNJ54LS244W	SNJ54LS244W
			SNJ54S240W	SNJ54S240W
			SNJ54S241W	SNJ54S241W
			SNJ54S244W	SNJ54S244W
	LCCC – FK	Tube	SNJ54LS240FK	SNJ54LS240FK
			SNJ54LS241FK	SNJ54LS241FK
			SNJ54LS244FK	SNJ54LS244FK
			SNJ54S240FK	SNJ54S240FK
			SNJ54S241FK	SNJ54S241FK
			SNJ54S244FK	SNJ54S244FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

schematics of inputs and outputs

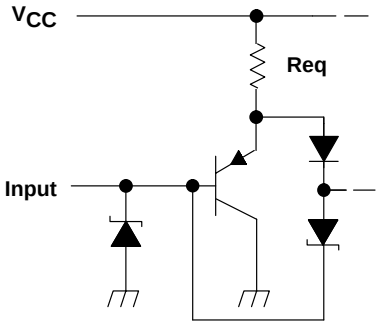
'LS240, 'LS241, 'LS244

EQUIVALENT OF EACH INPUT



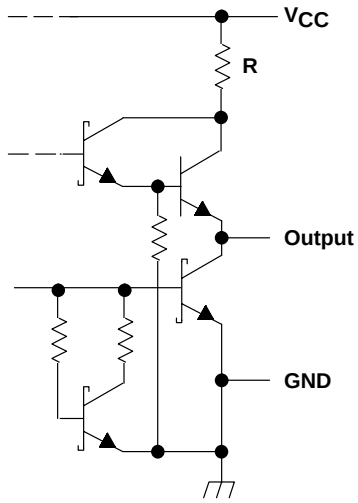
'S240, 'S241, 'S244

EQUIVALENT OF EACH INPUT



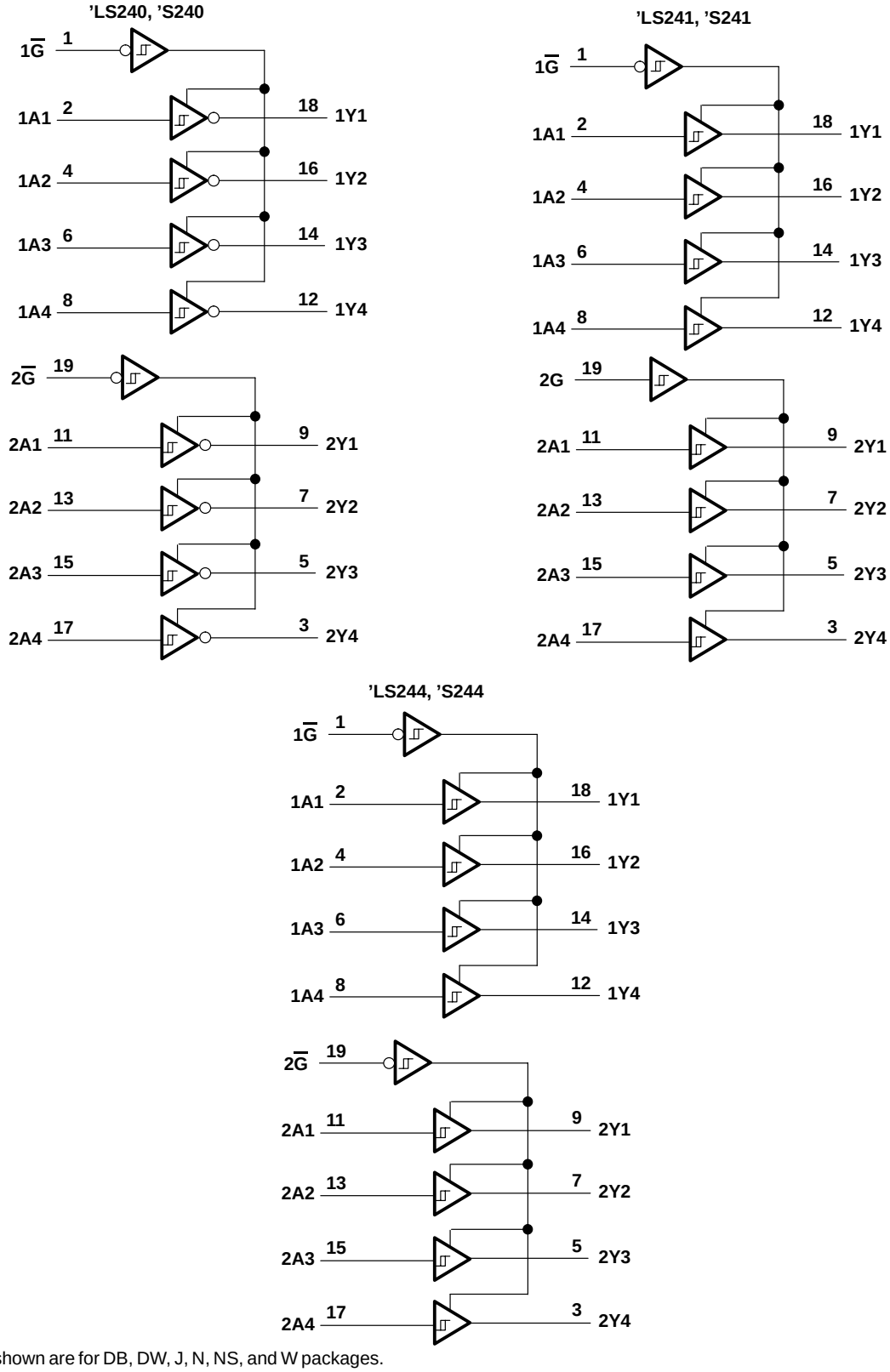
G and $\overline{G}$ inputs: R_{eq} = 2 kΩ NOM
A inputs: R_{eq} = 2.8 kΩ NOM

TYPICAL OF ALL OUTPUTS



'LS240. 'LS241, 'LS244: R = 50 Ω NOM
'S240, 'S241, S244: R = 25 Ω NOM

logic diagram



Pin numbers shown are for DB, DW, J, N, NS, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage, V_I: 'LS . . . . . 7 V
'S . . . . . 5.5 V
Off-state output voltage . . . . . 5.5 V
Package thermal impedance, θ_{JA} (see Note 2): DB package . . . . . 70°C/W
DW package . . . . . 58°C/W
N package . . . . . 69°C/W
NS package . . . . . 60°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Voltage values are with respect to network ground terminal.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

		SN54LS'			SN74LS'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			–12			–15	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	–55		125	0		70	°C

NOTE 1: Voltage values are with respect to network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			SN54LS'			SN74LS'			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN, I_I = –18 mA					–1.5			–1.5	V
Hysteresis ($V_{T+} - V_{T-}$)	V_{CC} = MIN			0.2	0.4		0.2	0.4		V
V_{OH}	V_{CC} = MIN, I_{OH} = –3 mA	V_{IH} = 2 V,	V_{IL} = MAX,	2.4	3.4		2.4	3.4		V
	V_{CC} = MIN, I_{OH} = MAX	V_{IH} = 2 V,	V_{IL} = 0.5 V,	2			2			
V_{OL}	V_{CC} = MIN, V_{IL} = MAX	V_{IH} = 2 V,	I_{OL} = 12 mA			0.4			0.4	V
			I_{OL} = 24 mA						0.5	
I_{OZH}	V_{CC} = MAX, V_{IL} = MAX	V_{IH} = 2 V,	V_O = 2.7 V			20			20	µA
I_{OZL}	V_{CC} = MAX, V_{IL} = MAX	V_{IH} = 2 V,	V_O = 0.4 V			–20			–20	µA
I_I	V_{CC} = MAX,	V_I = 7 V				0.1			0.1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.7 V				20			20	µA
I_{IL}	V_{CC} = MAX,	V_{IL} = 0.4 V				–0.2			–0.2	mA
I_{OS}§	V_{CC} = MAX,			–40		–225	–40		–225	mA
I_{CC}	V_{CC} = MAX, Output open	Outputs high	All		17	27		17	27	mA
		Outputs low	'LS240		26	44		26	44	
			'LS241, 'LS244		27	46		27	46	
		Outputs disabled	'LS240		29	50		29	50	
			'LS241, 'LS244		32	54		32	54	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Figure 1)

PARAMETER	TEST CONDITIONS		'LS240			'LS241, 'LS244			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	R_L = 667 Ω,	C_L = 45 pF		9	14		12	18	ns
t_{PHL}				12	18		12	18	
t_{PZL}	R_L = 667 Ω,	C_L = 45 pF		20	30		20	30	ns
t_{PZH}				15	23		15	23	
t_{PLZ}	R_L = 667 Ω,	C_L = 5 pF		10	20		10	20	ns
t_{PHZ}				15	25		15	25	

recommended operating conditions

		SN54S'			SN74S'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			–12			–15	mA
I_{OL}	Low-level output current			48			64	mA
	External resistance between any input and V_{CC} or ground			40			40	kΩ
T_A	Operating free-air temperature (see Note 3)	–55		125	0		70	°C

NOTES: 1. Voltage values are with respect to network ground terminal.
3. An SN54S241J operating at free-air temperature above 116°C requires a heat sink that provides a thermal resistance from case to free air, $R_{\theta CA}$, of not more that 40°C/W.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

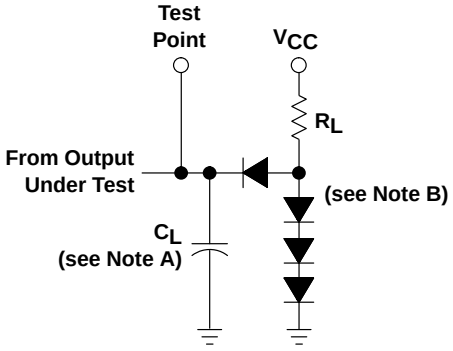
PARAMETER	TEST CONDITIONS†			SN54S'			SN74S'			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN, I_I = –18 mA					–1.2			–1.2	V
Hysteresis ($V_{T+} - V_{T-}$)	V_{CC} = MIN			0.2	0.4		0.2	0.4		V
V_{OH}	V_{CC} = MIN, I_{OH} = –1 mA	V_{IH} = 2 V,	V_{IL} = 0.8 V,				2.7			V
	V_{CC} = MIN, I_{OH} = –3 mA	V_{IH} = 2 V,	V_{IL} = 0.8 V,	2.4	3.4		2.4	3.4		
	V_{CC} = MIN, I_{OH} = MAX	V_{IH} = 2 V,	V_{IL} = 0.5 V,	2			2			
V_{OL}	V_{CC} = MIN, I_{OL} = MAX	V_{IH} = 2 V,	V_{IL} = 0.8 V,			0.55			0.55	V
I_{OZH}	V_{CC} = MAX, V_{IL} = 0.8 V	V_{IH} = 2 V,	V_O = 2.4 V			50			50	µA
I_{OZL}	V_{CC} = MAX, V_{IL} = 0.8 V	V_{IH} = 2 V,	V_O = 0.5 V			–50			–50	µA
I_I	V_{CC} = MAX,	V_I = 5.5 V				1			1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.7 V				50			50	µA
I_{IL}	V_{CC} = MAX,	V_I = 0.5 V	Any A			–400			–400	µA
			Any G			–2			–2	mA
I_{OS}§	V_{CC} = MAX			–50		–225	–50		–225	mA
I_{CC}	V_{CC} = MAX, Output open	Outputs high	’S240		80	123		80	135	mA
			’S241,’S244		95	147		95	160	
		Outputs low	’S240		100	145		100	150	
			’S241, ’S244		120	170		120	180	
		Outputs disabled	’S240		100	145		100	150	
			’S241, ’S244		120	170		120	180	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

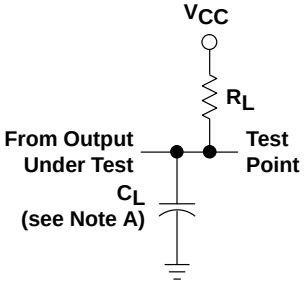
switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Figure 2)

PARAMETER	TEST CONDITIONS		'S240			'S241, 'S244			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	R_L = 90 Ω,	C_L = 50 pF		4.5	7		6	9	ns
t_{PHL}				4.5	7		6	9	
t_{PZL}	R_L = 90 Ω,	C_L = 50 pF		10	15		10	15	ns
t_{PZH}				6.5	10		8	12	
t_{PLZ}	R_L = 90 Ω,	C_L = 5 pF		10	15		10	15	ns
t_{PHZ}				6	9		6	9	

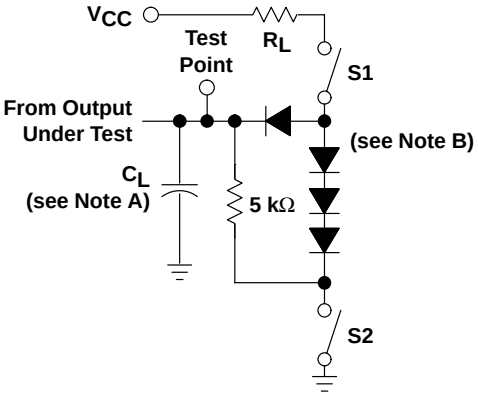
PARAMETER MEASUREMENT INFORMATION
SERIES 54LS/74LS DEVICES



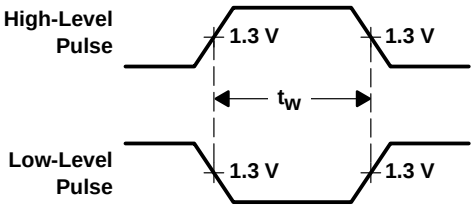
LOAD CIRCUIT
FOR 2-STATE TOTEM-POLE OUTPUTS



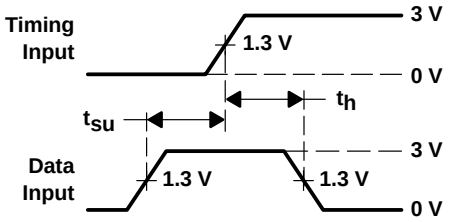
LOAD CIRCUIT
FOR OPEN-COLLECTOR OUTPUTS



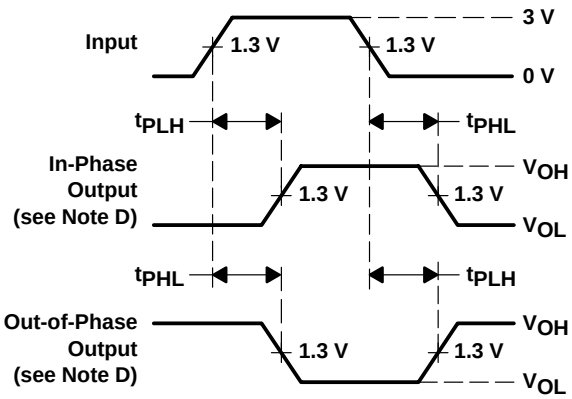
LOAD CIRCUIT
FOR 3-STATE OUTPUTS



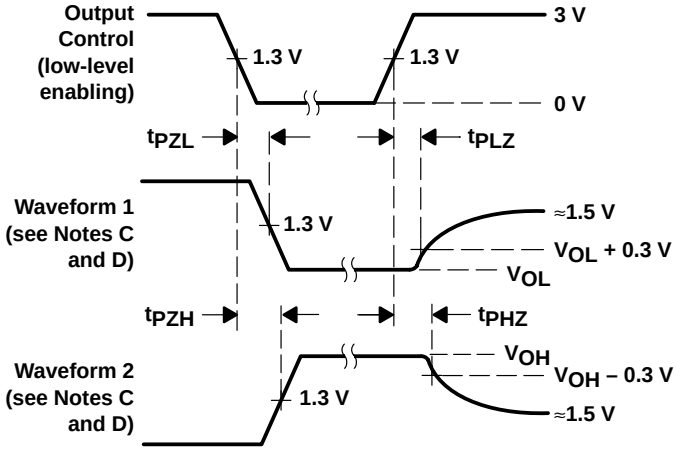
VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

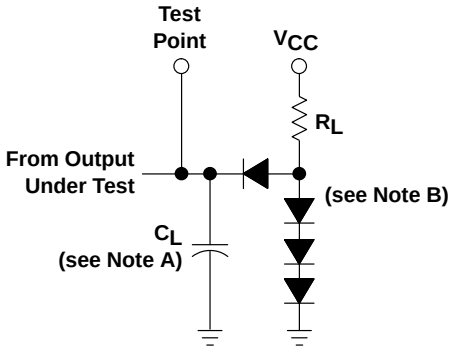


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

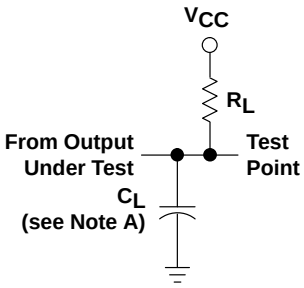
NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064 or equivalent.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. S1 and S2 are closed for t_{PLH}, t_{PHL}, t_{PHZ}, and t_{PLZ}; S1 is open and S2 is closed for t_{PZH}; S1 is closed and S2 is open for t_{PZL}.
E. Phase relationships between inputs and outputs have been chosen arbitrarily for these examples.
F. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O \approx 50\ \Omega$, $t_r \le 15$ ns, $t_f \le 6$ ns.
G. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

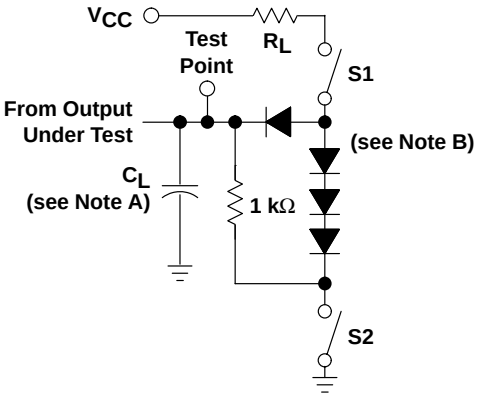
PARAMETER MEASUREMENT INFORMATION
SERIES 54S/74S DEVICES



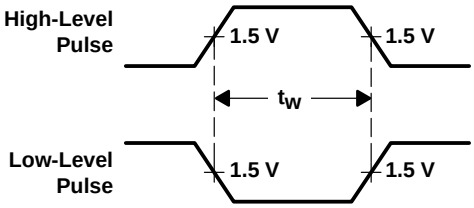
LOAD CIRCUIT
FOR 2-STATE TOTEM-POLE OUTPUTS



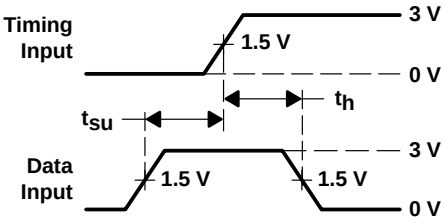
LOAD CIRCUIT
FOR OPEN-COLLECTOR OUTPUTS



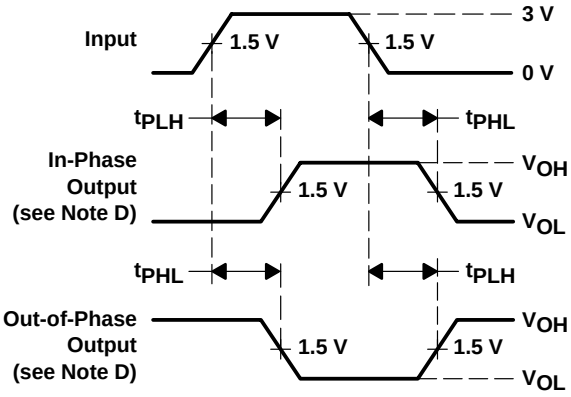
LOAD CIRCUIT
FOR 3-STATE OUTPUTS



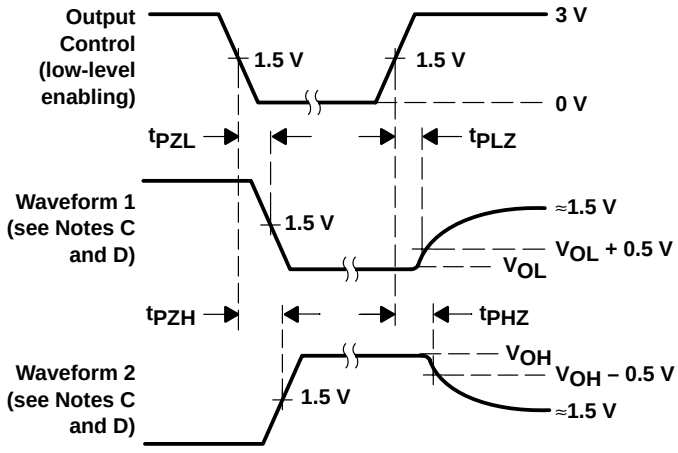
VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

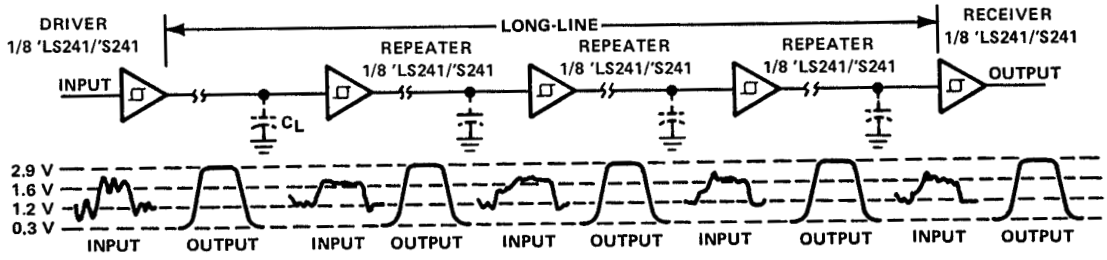


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

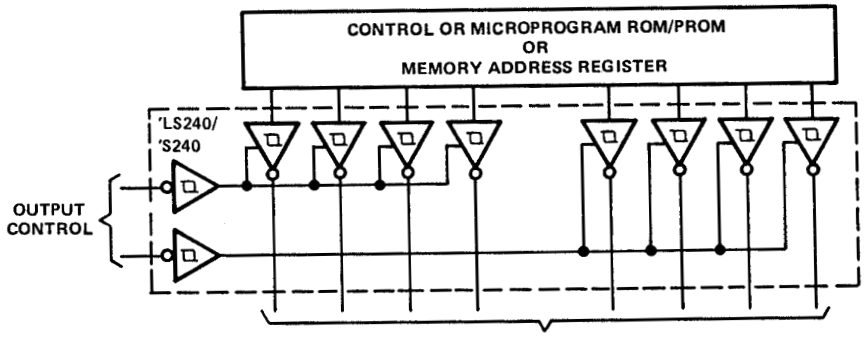
NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064 or equivalent.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. S1 and S2 are closed for t_{PLH}, t_{PHL}, t_{PHZ}, and t_{PLZ}; S1 is open and S2 is closed for t_{PZH}; S1 is closed and S2 is open for t_{PZL}.
E. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O \approx 50\ \Omega$; t_r and $t_f \leq 7$ ns for Series 54/74 devices and t_r and $t_f \leq 2.5$ ns for Series 54S/74S devices.
F. The outputs are measured one at a time with one input transition per measurement.

Figure 2. Load Circuits and Voltage Waveforms

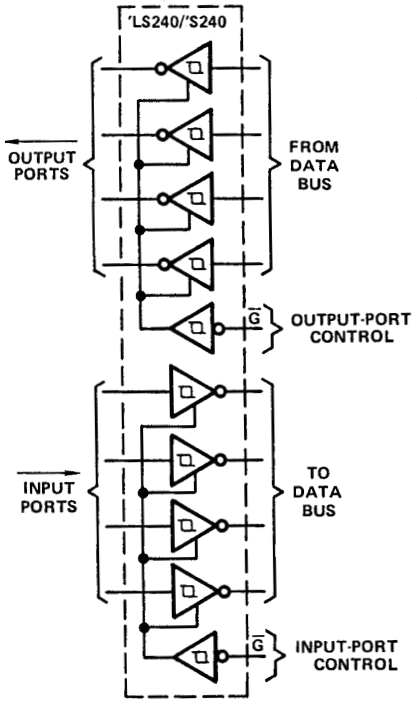
APPLICATION INFORMATION



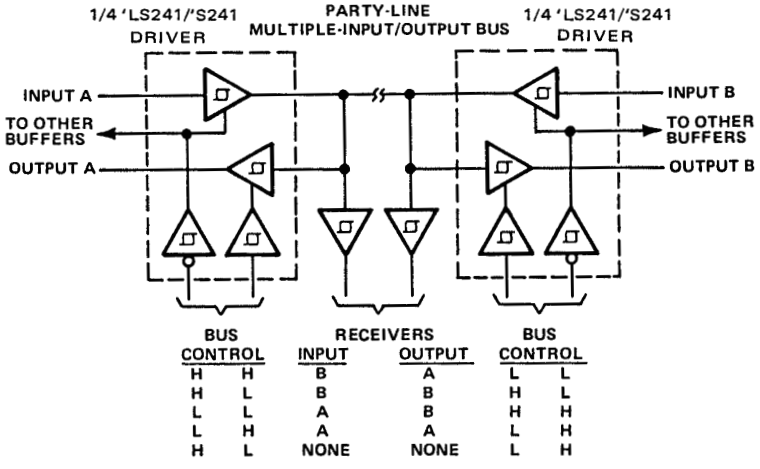
'LS241, 'S241 USED AS REPEATER/LEVEL RESTORER



'LS240/'S240 USED AS SYSTEM AND/OR MEMORY BUS DRIVER–4-BIT ORGANIZATION CAN BE APPLIED TO HANDLE BINARY OR BCD



INDEPENDENT 4-BIT BUS DRIVERS/RECEIVERS IN A SINGLE PACKAGE



BUS CONTROL		RECEIVERS INPUT	RECEIVERS OUTPUT	BUS CONTROL	
H	H	B	A	L	L
H	L	B	B	H	L
L	L	A	B	H	H
L	H	A	A	L	H
H	L	NONE	NONE	L	H

PARTY-LINE BUS SYSTEM WITH MULTIPLE INPUTS, OUTPUTS, AND RECEIVERS

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
5962-7801201VRA	ACTIVE	CDIP	J	20	1	TBD	Call TI	Level-NC-NC-NC
5962-7801201VSA	ACTIVE	CFP	W	20	1	TBD	Call TI	Level-NC-NC-NC
7705701RA	ACTIVE	CDIP	J	20	1	TBD	Call TI	Level-NC-NC-NC
7705701SA	ACTIVE	CFP	W	20	1	TBD	Call TI	Level-NC-NC-NC
78012012A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Level-NC-NC-NC
7801201RA	ACTIVE	CDIP	J	20	1	TBD	Call TI	Level-NC-NC-NC
7801201SA	ACTIVE	CFP	W	20	1	TBD	Call TI	Level-NC-NC-NC
JM38510/32401B2A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Level-NC-NC-NC
JM38510/32401BRA	ACTIVE	CDIP	J	20	1	TBD	Call TI	Level-NC-NC-NC
JM38510/32401BSA	ACTIVE	CFP	W	20	1	TBD	Call TI	Level-NC-NC-NC
JM38510/32402B2A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Level-NC-NC-NC
JM38510/32402BRA	ACTIVE	CDIP	J	20	1	TBD	Call TI	Level-NC-NC-NC
JM38510/32402BSA	ACTIVE	CFP	W	20	1	TBD	Call TI	Level-NC-NC-NC
JM38510/32403B2A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Level-NC-NC-NC
JM38510/32403BRA	ACTIVE	CDIP	J	20	1	TBD	Call TI	Level-NC-NC-NC
JM38510/32403BSA	ACTIVE	CFP	W	20	1	TBD	Call TI	Level-NC-NC-NC
JM38510/32403SRA	ACTIVE	CDIP	J	20	1	TBD	Call TI	Level-NC-NC-NC
JM38510/32403SSA	ACTIVE	CFP	W	20	1	TBD	Call TI	Level-NC-NC-NC
SN54LS240J	ACTIVE	CDIP	J	20	1	TBD	Call TI	Level-NC-NC-NC
SN54LS241J	ACTIVE	CDIP	J	20	1	TBD	Call TI	Level-NC-NC-NC
SN54LS244J	ACTIVE	CDIP	J	20	1	TBD	Call TI	Level-NC-NC-NC
SN54S240J	ACTIVE	CDIP	J	20	1	TBD	Call TI	Level-NC-NC-NC
SN54S241J	ACTIVE	CDIP	J	20	1	TBD	Call TI	Level-NC-NC-NC
SN54S244J	ACTIVE	CDIP	J	20	1	TBD	Call TI	Level-NC-NC-NC
SN74LS240DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS240DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS240DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS240J	OBSOLETE	CDIP	J	20		TBD	Call TI	Call TI
SN74LS240N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74LS240N3	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI
SN74LS240NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74LS240NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS240NSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS240NSRG4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS241DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS241DWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS &	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
						no Sb/Br)		
SN74LS241DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS241DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS241J	OBSOLETE	CDIP	J	20		TBD	Call TI	Call TI
SN74LS241N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74LS241N3	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI
SN74LS241NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74LS241NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS241NSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS244DBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS244DBRE4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS244DBRG4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS244DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS244DWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS244DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS244DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS244DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS244DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS244J	OBSOLETE	CDIP	J	20		TBD	Call TI	Call TI
SN74LS244N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74LS244N3	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI
SN74LS244NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74LS244NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS244NSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS244NSRG4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S240DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S240DWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S240DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SN74S240DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S240N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74S240N3	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI
SN74S240NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74S241DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S241DWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S241DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S241DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S241J	OBSOLETE	CDIP	J	20		TBD	Call TI	Call TI
SN74S241N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74S241N3	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI
SN74S241NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74S244DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S244DWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S244DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S244DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S244J	OBSOLETE	CDIP	J	20		TBD	Call TI	Call TI
SN74S244N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74S244N3	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI
SN74S244NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SNJ54LS240FK	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Level-NC-NC-NC
SNJ54LS240J	ACTIVE	CDIP	J	20	1	TBD	Call TI	Level-NC-NC-NC
SNJ54LS240W	ACTIVE	CFP	W	20	1	TBD	Call TI	Level-NC-NC-NC
SNJ54LS241FK	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Level-NC-NC-NC
SNJ54LS241J	ACTIVE	CDIP	J	20	1	TBD	Call TI	Level-NC-NC-NC
SNJ54LS241W	ACTIVE	CFP	W	20	1	TBD	Call TI	Level-NC-NC-NC
SNJ54LS244FK	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Level-NC-NC-NC
SNJ54LS244J	ACTIVE	CDIP	J	20	1	TBD	Call TI	Level-NC-NC-NC
SNJ54LS244W	ACTIVE	CFP	W	20	1	TBD	Call TI	Level-NC-NC-NC
SNJ54S240FK	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Level-NC-NC-NC
SNJ54S240J	ACTIVE	CDIP	J	20	1	TBD	Call TI	Level-NC-NC-NC
SNJ54S240W	ACTIVE	CFP	W	20	1	TBD	Call TI	Level-NC-NC-NC
SNJ54S241FK	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Level-NC-NC-NC

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
SNJ54S241J	ACTIVE	CDIP	J	20	1	TBD	Call TI	Level-NC-NC-NC
SNJ54S241W	ACTIVE	CFP	W	20	1	TBD	Call TI	Level-NC-NC-NC
SNJ54S244FK	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Level-NC-NC-NC
SNJ54S244J	ACTIVE	CDIP	J	20	1	TBD	Call TI	Level-NC-NC-NC
SNJ54S244W	ACTIVE	CFP	W	20	1	TBD	Call TI	Level-NC-NC-NC

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

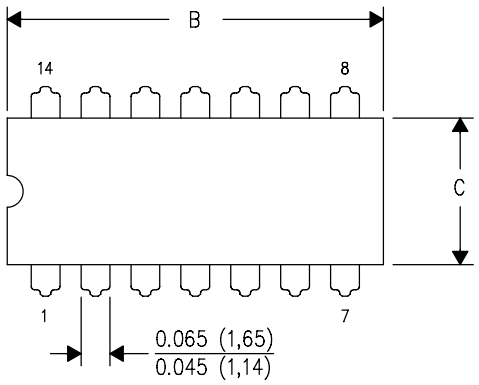
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

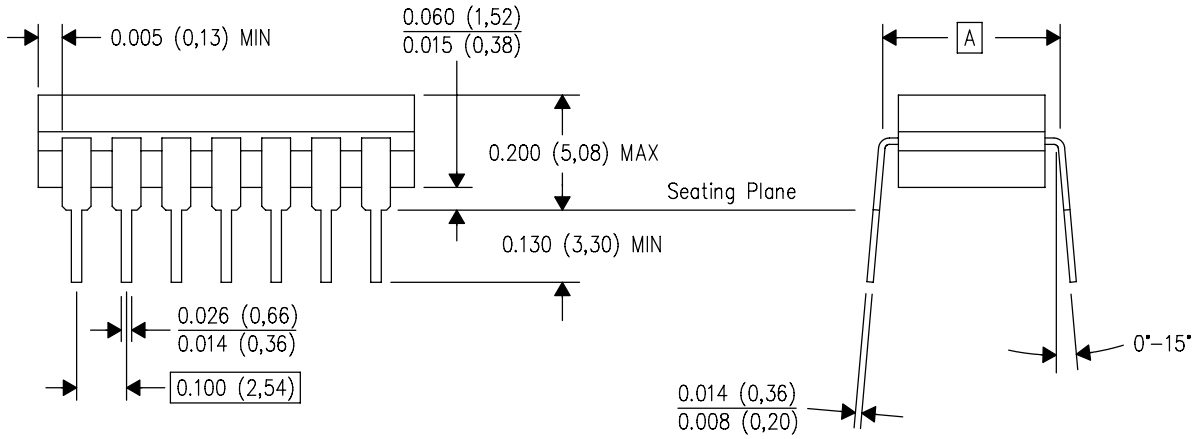
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



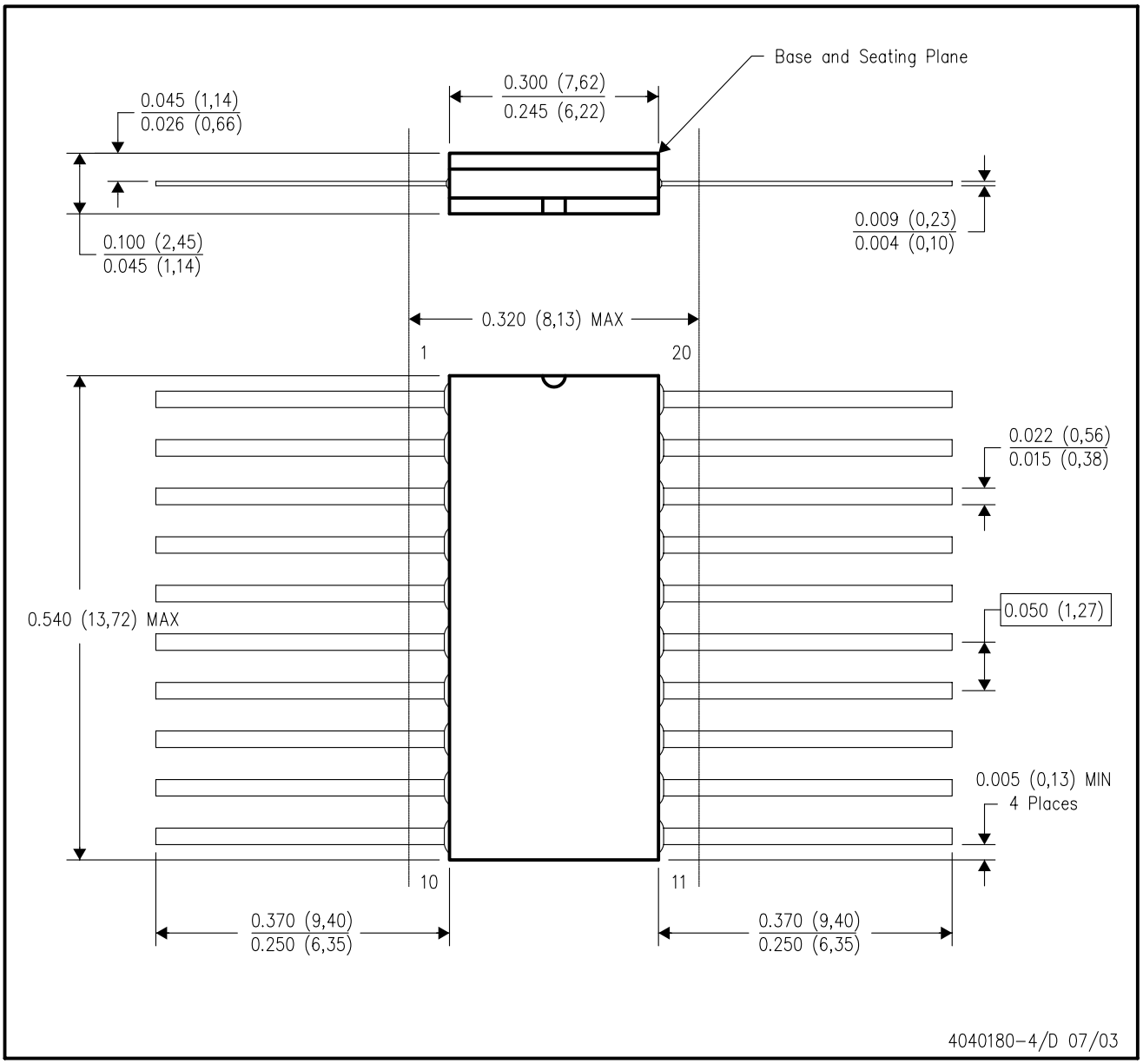
DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

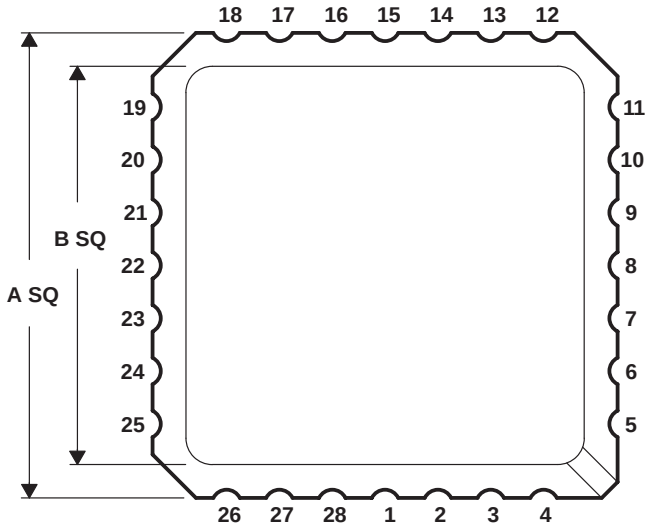
W (R–GDFP–F20) CERAMIC DUAL FLATPACK



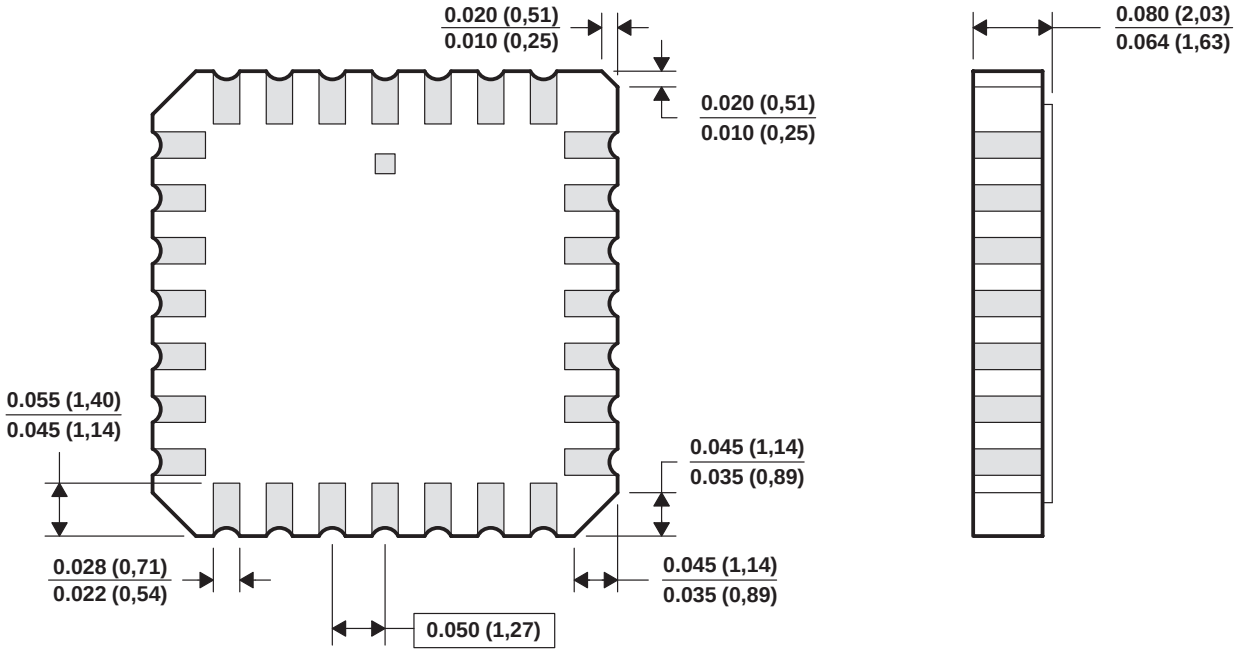
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within Mil–Std 1835 GDFP2–F20

FK (S-CQCC-N)** **LEADLESS CERAMIC CHIP CARRIER**

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.739 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



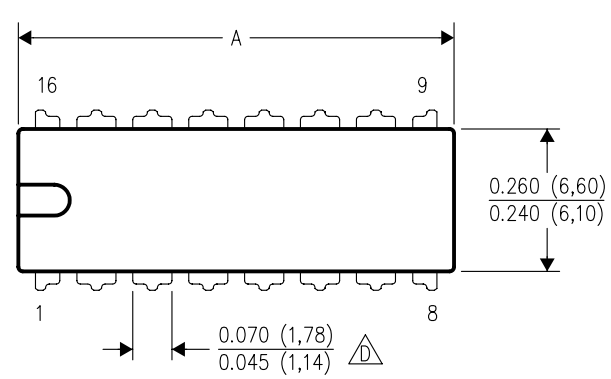
4040140/D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. Falls within JEDEC MS-004

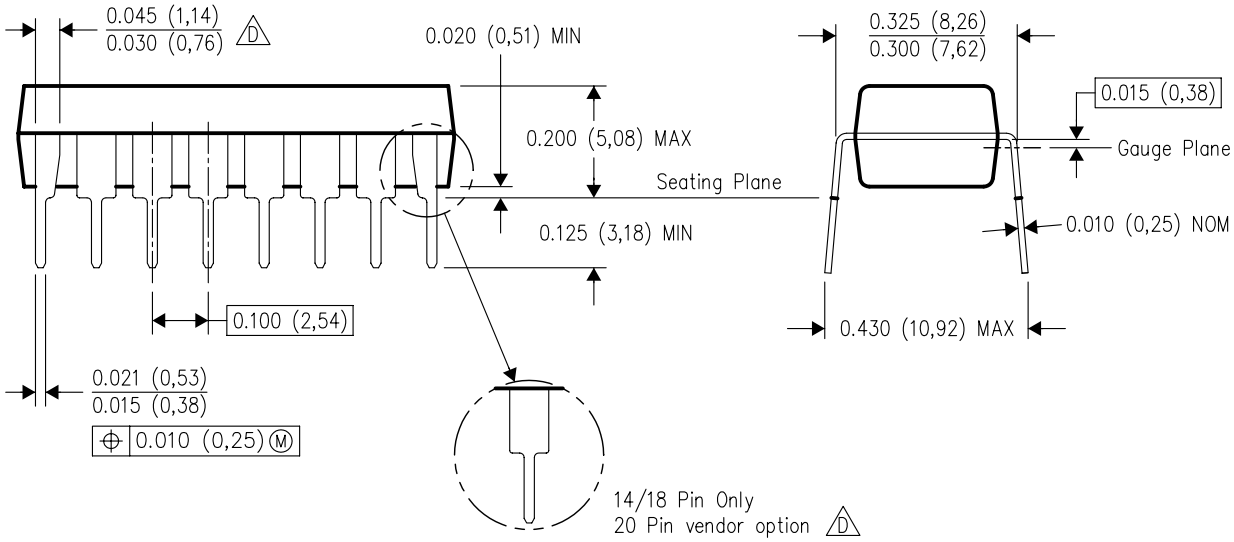
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



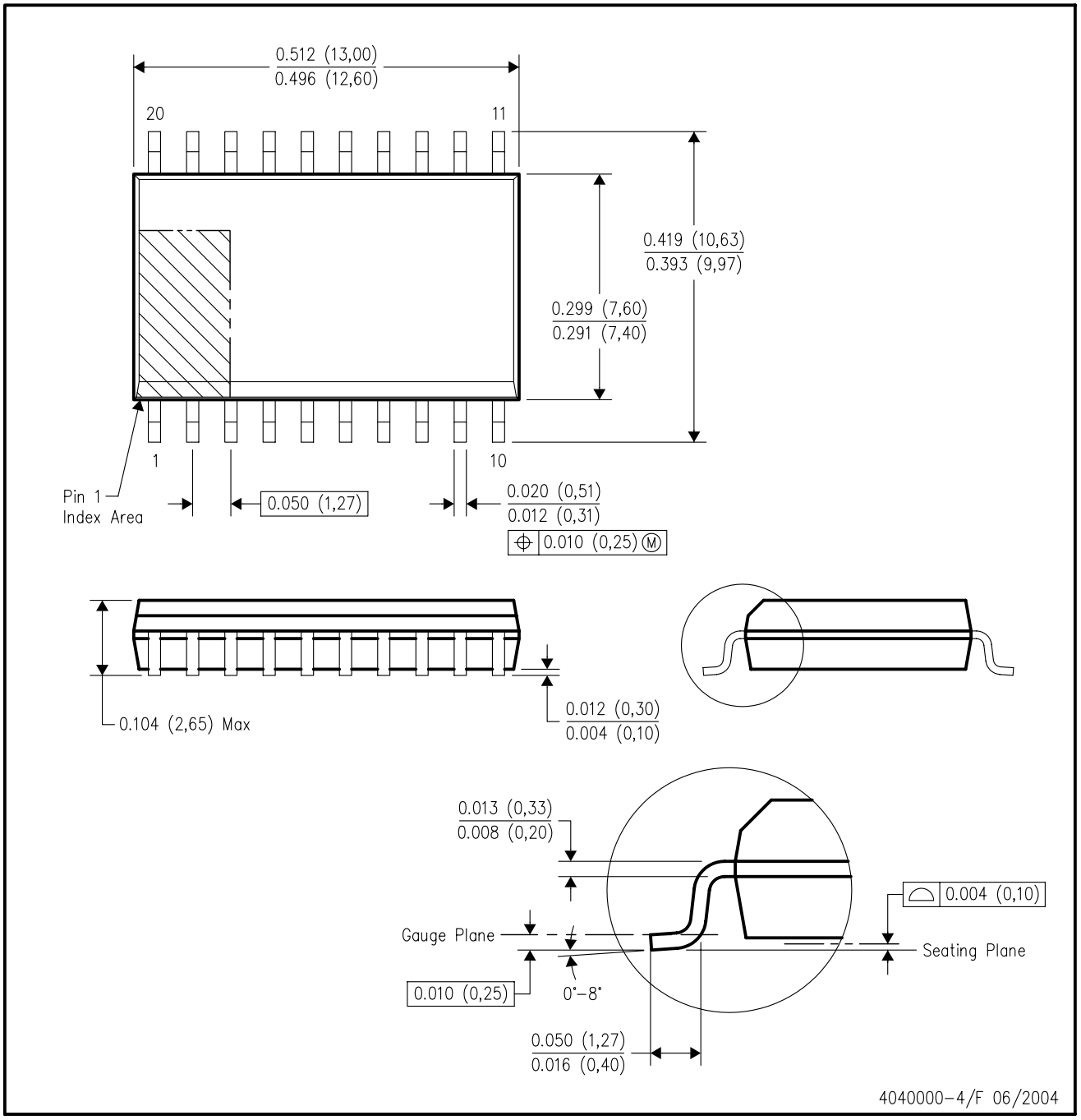
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW (R–PDSO–G20) PLASTIC SMALL–OUTLINE PACKAGE

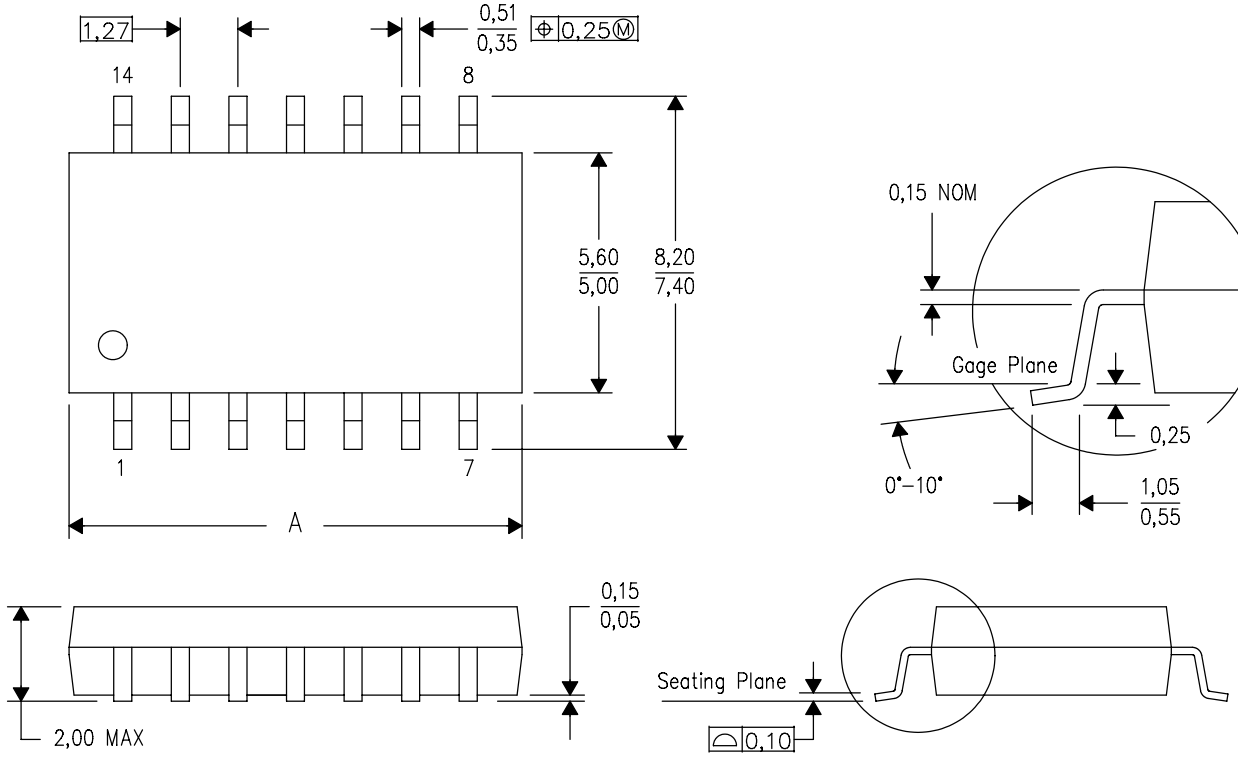


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AC.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

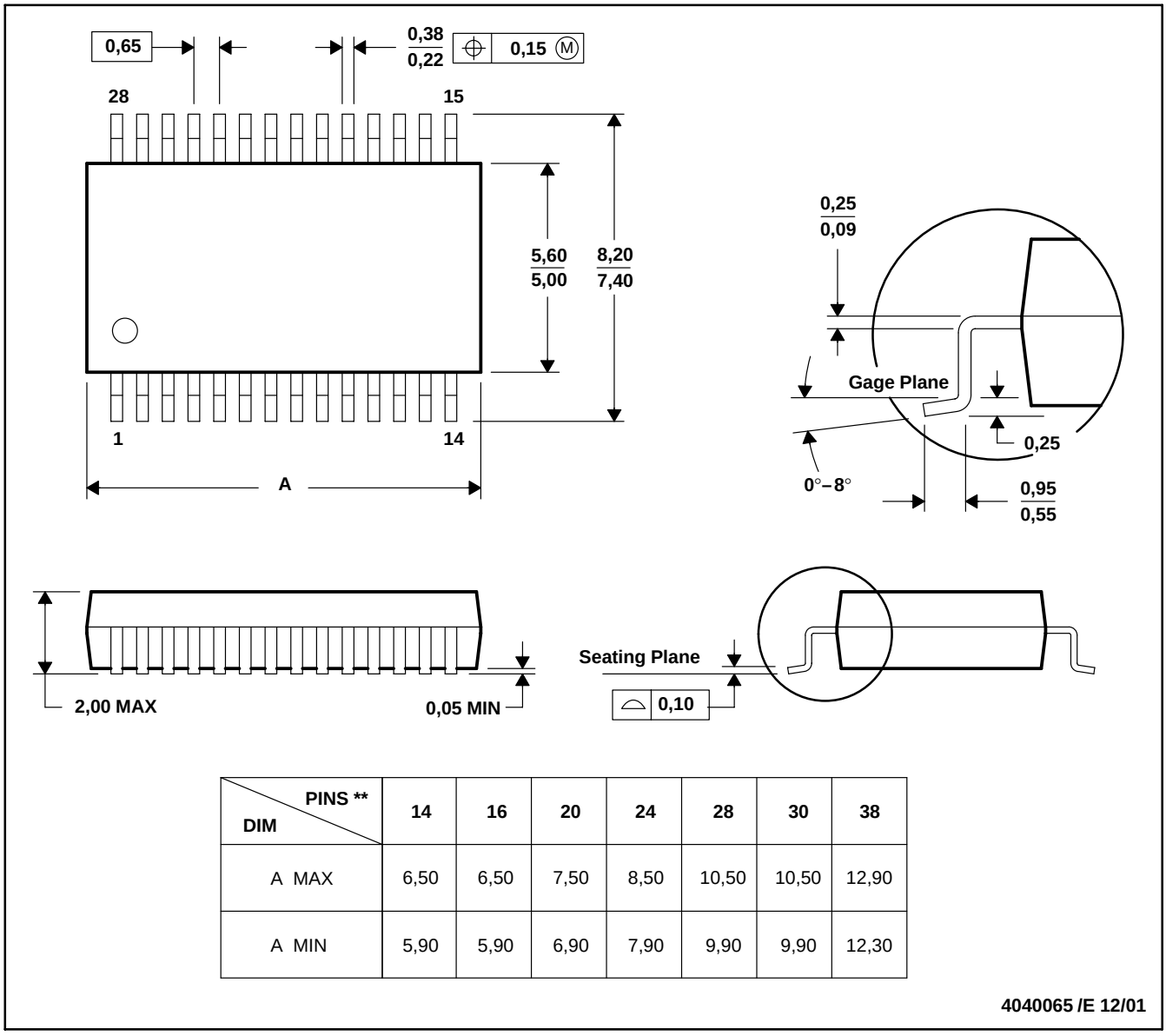
4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

MSSO002E – JANUARY 1995 – REVISED DECEMBER 2001

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

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Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
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		Video & Imaging	www.ti.com/video
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Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265

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SN74LS240, Status: ACTIVE

Octal buffers and line drivers

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Features | Samples | Technical Documents
Quality & Pb-Free Data | Pricing/Packaging | Applications Notes
Related Products | Inventory | Simulation Models
Tools & Software | Symbols/Footprints | Reference Designs

Refine Your Selection
- Logic: Inverting Buffers Drivers

Support
- KnowledgeBase
- Contact Technical Supp
- TI Cross Reference
- Training
- Part Marking Lookup
- Part Number Nomencla

Datasheet

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Octal Buffers and Line Drivers With 3-State Outputs (Rev. B) (sn74ls240.pdf, 648 KB)
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	SN54LS240	SN74LS240
Voltage Nodes(V)	5	5
Vcc range(V)	4.5 to 5.5	4.75 to 5.25
Input Level	TTL	TTL
Output Level	TTL	TTL
No. of Outputs	8	8
Output Drive(mA)		-15/24
tpd max(ns)		18
Static Current		35.5
Logic	Inv	Inv
	Samples	Samples
	Inventory	Inventory

Product Information

Features

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3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
PNP Inputs Reduce DC Loading
Hysteresis at Inputs Improves Noise Margins

Description

These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The designer has a choice of selected combinations of inverting and noninverting outputs, symmetrical, active-low output-control (G)\ inputs, and complementary output-control (G and G\) inputs. These devices feature high fan-out, improved fan-in, and 400-mV noise margin. The SN74LS' and SN74S' devices can be used to drive terminated lines down to 133 · .

Pricing/Packaging/CAD Design Tools/Samples

			Price	Packaging			CAD Design Tools	Samples
Device	Status	Temp (°C)	Budget Price ($US) | QTY	Industry Standard (TI Pkg) | Pins	Top Side Marking	Standard Pack Quantity	Footprints	Samples
SN74LS240DW	ACTIVE	0 to 70	0.44 | 1KU	SOIC (DW) | 20	View	25		Purchase Samples
SN74LS240DWR	ACTIVE	0 to 70	0.44 | 1KU	SOIC (DW) | 20	View	2000		Purchase Samples
SN74LS240DWRE4	ACTIVE	0 to 70	0.44 | 1KU	SOIC (DW) | 20	View	2000		Purchase Samples
SN74LS240J	OBSOLETE	0 to 70		CDIP (J) | 20				Not Available
SN74LS240N	ACTIVE	0 to 70	0.44 | 1KU	PDIP (N) | 20	View	20		Purchase Samples
SN74LS240N3	OBSOLETE	0 to 70		PDIP (N) | 20	View			Not Available
SN74LS240NE4	ACTIVE		0.42 | 1KU	PDIP (N) | 20	View	20		Purchase Samples
SN74LS240NSR	ACTIVE	0 to 70	0.44 | 1KU	SO (NS) | 20	View	2000		Purchase Samples
SN74LS240NSRE4	ACTIVE	0 to 70	0.44 | 1KU	SO (NS) | 20	View	2000		Purchase Samples
SN74LS240NSRG4	ACTIVE	0 to 70	0.48 | 1KU	SO (NS) | 20	View	2000		Purchase Samples

Inventory

View all Distributors

Choose a Region

	TI Inventory Status			Reported Distributor Inventory			
SN74LS240DW	As of 9:10 AM GMT, 29 Nov 2005			As of 9:10 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY | Date	Lead Time	Region	Company	In Stock	Purchase
	0*	675 | 12 Dec	8 Weeks	Americas	DigiKey	452	
		>10k | 30 Jan			Newark InOne	325	
				Europe	Abacus Polar	630	
					Arrow Southern Europe	>1k	
					EBV Elektronik	>1k	
					Spoerle	499	
SN74LS240DWR	As of 9:10 AM GMT, 29 Nov 2005			As of 9:10 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY | Date	Lead Time	Region	Company	In Stock	Purchase
	0*	>10k | 30 Jan	9 Weeks	Americas	DigiKey	908	
				Europe	EBV Elektronik	>1k	
SN74LS240DWRE4	As of 9:10 AM GMT, 29 Nov 2005			As of 9:10 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY | Date	Lead Time	Region	Company	In Stock	Purchase
	0*	>10k | 30 Jan	9 Weeks	None Reported View Distributors			
SN74LS240N	As of 9:10 AM GMT, 29 Nov 2005			As of 9:10 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY | Date	Lead Time	Region	Company	In Stock	Purchase

	8160*	>10k | 12 Dec	4 Weeks	Americas	Avnet	>1k	
					DigiKey	>1k	
					Newark InOne	>1k	
				Europe	Abacus Polar	560	
					Arrow Northern Europe	>1k	
					Arrow Southern Europe	>1k	
					Avnet-SILICA	>1k	
					EBV Elektronik	>1k	

SN74LS240NE4	As of 9:10 AM GMT, 29 Nov 2005			As of 9:10 AM GMT, 29 Nov 2005			
	In Stock	**In Progress QTY | Date**	**Lead Time**	**Region**	**Company**	**In Stock**	**Purchase**
	0*	3420 | 12 Dec	10 Weeks	None Reported View Distributors			
		>10k | 16 Jan					

SN74LS240NSR	As of 9:10 AM GMT, 29 Nov 2005			As of 9:10 AM GMT, 29 Nov 2005			
	In Stock	**In Progress QTY | Date**	**Lead Time**	**Region**	**Company**	**In Stock**	**Purchase**
	0*	2 | 7 Dec	4 Weeks	None Reported View Distributors			
		4695 | 16 Dec					
		>10k | 30 Dec					

SN74LS240NSRE4	As of 9:10 AM GMT, 29 Nov 2005			As of 9:10 AM GMT, 29 Nov 2005			
	In Stock	**In Progress QTY | Date**	**Lead Time**	**Region**	**Company**	**In Stock**	**Purchase**
	0*	4673 | 16 Dec	8 Weeks	None Reported View Distributors			
		>10k | 30 Dec					

SN74LS240NSRG4	As of 9:10 AM GMT, 29 Nov 2005			As of 9:10 AM GMT, 29 Nov 2005			
	In Stock	**In Progress QTY | Date**	**Lead Time**	**Region**	**Company**	**In Stock**	**Purchase**
	0*	4705 | 19 Dec	8 Weeks	None Reported View Distributors			
		>10k | 3 Jan					

* Our information is updated daily, so please check back with us soon if this does not meet your needs. You may also contact your TI Authorized Distributor, including those listed above, for real time stock information.

** Lead time information is not available at this time. However, our information is updated daily so please check back with us soon. Please contact your preferred TI Authorized Distributor for additional information.

Quality & Lead (Pb)-Free Data

	Product Content				MTBF/FIT Rate
Device	**Eco Plan***	**Lead/Ball Finish**	**MSL Rating/Peak Reflow**	**Details**	**Details**
SN74LS240DW	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74LS240DWR	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74LS240DWRE4	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74LS240N	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC	View	View
SN74LS240NE4	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC	View	View
SN74LS240NSR	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74LS240NSRE4	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74LS240NSRG4	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View

* The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please click on the Product Content Details "View" link in the table above for the latest availability information and additional product content details.

If the information you are requesting is not available online at this time, contact one of our Product Information Centers regarding the availability of this information.

Technical Documents

Datasheets

Keep track of what's new

Octal Buffers and Line Drivers With 3-State Outputs (Rev. B) (sn74ls240.pdf, 648 KB)
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Application Notes

Semiconductor Packing Material Electrostatic Discharge (ESD) Protection (szza047.htm, 9 KB)
08 Jul 2004 Abstract

Shelf-Life Evaluation of Lead-Free Component Finishes (szza046.htm, 9 KB)
24 May 2004 Abstract

Understanding and Interpreting Standard-Logic Data Sheets (Rev. B) (szza036b.htm, 8 KB)
28 May 2003 Abstract

TI IBIS File Creation, Validation, and Distribution Processes (szza034.htm, 9 KB)
29 Aug 2002 Abstract

Designing With Logic (Rev. C) (sdya009c.htm, 9 KB)
01 Jun 1997 Abstract

Designing with the SN54/74LS123 (Rev. A) (sdla006a.htm, 9 KB)
01 Mar 1997 Abstract

Live Insertion (sdya012.htm, 9 KB)
01 Oct 1996 Abstract

Input and Output Characteristics of Digital Integrated Circuits (sdya010.htm, 9 KB)
01 Oct 1996 Abstract

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User Guides

LOGIC Pocket Data Book (scyd013.pdf, 4835 KB)
05 Dec 2002 Download

Simulation Models

IBIS Model

IBIS Model of SN74LS240 (Rev. B) (sdlm007b.ibs, 38 KB)
22 Nov 2004 ibis / zip

More Literature

Logic Selection Guide 2005 (Rev. X) (sdyu001x.pdf, 6909 KB)
15 Mar 2005 Download

Military Semiconductors Selection Guide 2004-2005 (Rev. D) (sgyc003d.pdf, 964 KB)
10 Aug 2004 Download

Logic Cross-Reference (Rev. A) (scyb017a.pdf, 2938 KB)
07 Oct 2003 Download

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