

# SN54390, SN54LS390, SN54393, SN54LS393 SN74390, SN74LS390, SN74393, SN74LS393 DUAL 4-BIT DECADE AND BINARY COUNTERS

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- Dual Versions of the Popular '90A, 'LS90 and '93A, 'LS93
- '390, 'LS390 . . . Individual Clocks for A and B Flip-Flops Provide Dual ÷ 2 and ÷ 5 Counters
- '393, 'LS393 . . . Dual 4-Bit Binary Counter with Individual Clocks
- All Have Direct Clear for Each 4-Bit Counter
- Dual 4-Bit Versions Can Significantly Improve System Densities by Reducing Counter Package Count by 50%
- Typical Maximum Count Frequency . . . 35 MHz
- Buffered Outputs Reduce Possibility of Collector Commutation

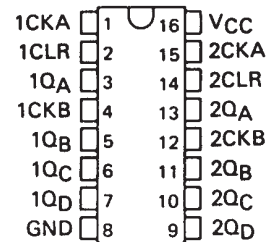
## description

Each of these monolithic circuits contains eight master-slave flip-flops and additional gating to implement two individual four-bit counters in a single package. The '390 and 'LS390 incorporate dual divide-by-two and divide-by-five counters, which can be used to implement cycle lengths equal to any whole and/or cumulative multiples of 2 and/or 5 up to divide-by-100. When connected as a bi-quinary counter, the separate divide-by-two circuit can be used to provide symmetry (a square wave) at the final output stage. The '393 and 'LS393 each comprise two independent four-bit binary counters each having a clear and a clock input. N-bit binary counters can be implemented with each package providing the capability of divide-by-256. The '390, 'LS390, '393, and 'LS393 have parallel outputs from each counter stage so that any submultiple of the input count frequency is available for system-timing signals.

Series 54 and Series 54LS circuits are characterized for operation over the full military temperature range of -55°C to 125°C; Series 74 and Series 74LS circuits are characterized for operation from 0°C to 70°C.

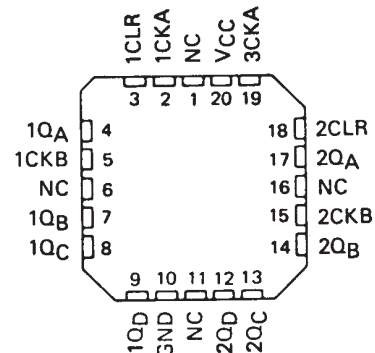
SN54390, SN54LS390 . . . J OR W PACKAGE  
SN74390 . . . N PACKAGE  
SN74LS390 . . . D OR N PACKAGE

(TOP VIEW)



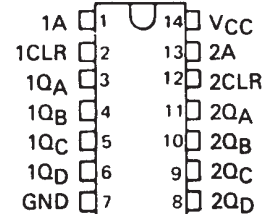
SN54LS390 . . . FK PACKAGE

(TOP VIEW)



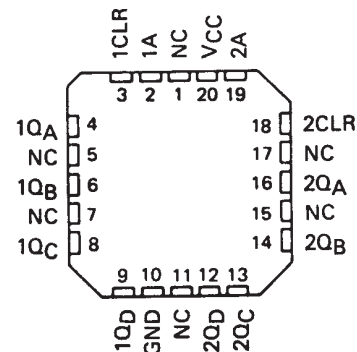
SN54393, SN54LS393 . . . J OR W PACKAGE  
SN74393 . . . N PACKAGE  
SN74LS393 . . . D OR N PACKAGE

(TOP VIEW)



SN54LS393 . . . FK PACKAGE

(TOP VIEW)



NC - No internal connection

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**'390, 'LS390  
BCD COUNT SEQUENCE  
(EACH COUNTER)  
(See Note A)**

COUNT	OUTPUT			
	Q <sub>D</sub>	Q <sub>C</sub>	Q <sub>B</sub>	Q <sub>A</sub>
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

**FUNCTION TABLES  
'390, 'LS390  
BI-QUINARY (5-2)  
(EACH COUNTER)  
(See Note B)**

COUNT	OUTPUT			
	Q <sub>A</sub>	Q <sub>D</sub>	Q <sub>C</sub>	Q <sub>B</sub>
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

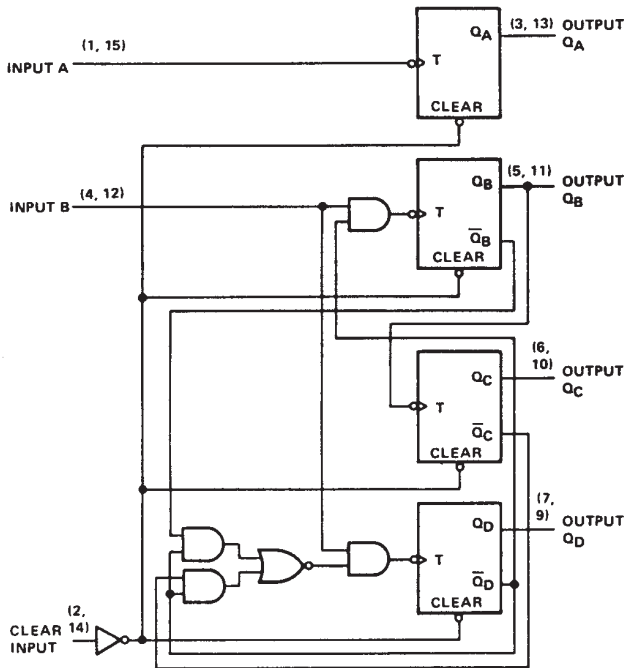
**'393, 'LS393  
COUNT SEQUENCE  
(EACH COUNTER)**

COUNT	OUTPUT			
	Q <sub>D</sub>	Q <sub>C</sub>	Q <sub>B</sub>	Q <sub>A</sub>
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

NOTES: A. Output Q<sub>A</sub> is connected to input B for BCD count.  
B. Output Q<sub>D</sub> is connected to input A for bi-quinary count.  
C. H = high level, L = low level.

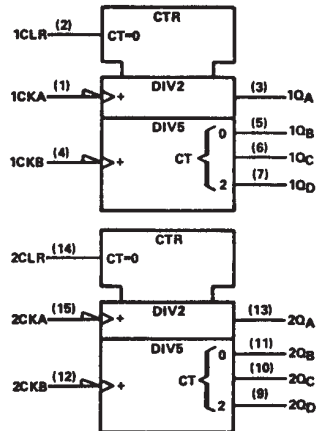
**logic diagrams (positive logic)**

**'390, 'LS390**

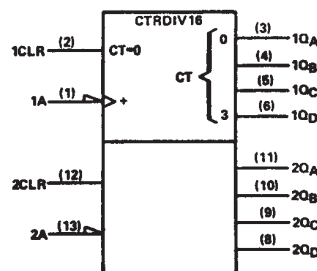


**logic symbols †**

**'390, 'LS390**



**'393, 'LS393**



†These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, N, and W packages.

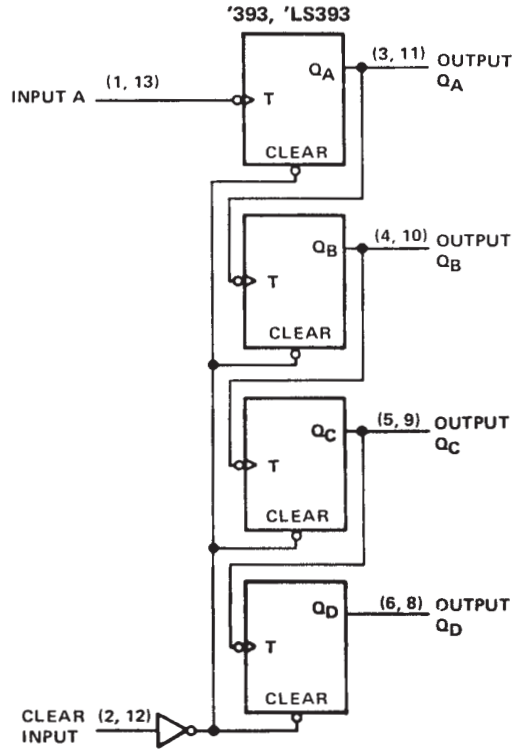


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SN54390, SN54LS390, SN54393, SN54LS393  
 SN74390, SN74LS390, SN74393, SN74LS393  
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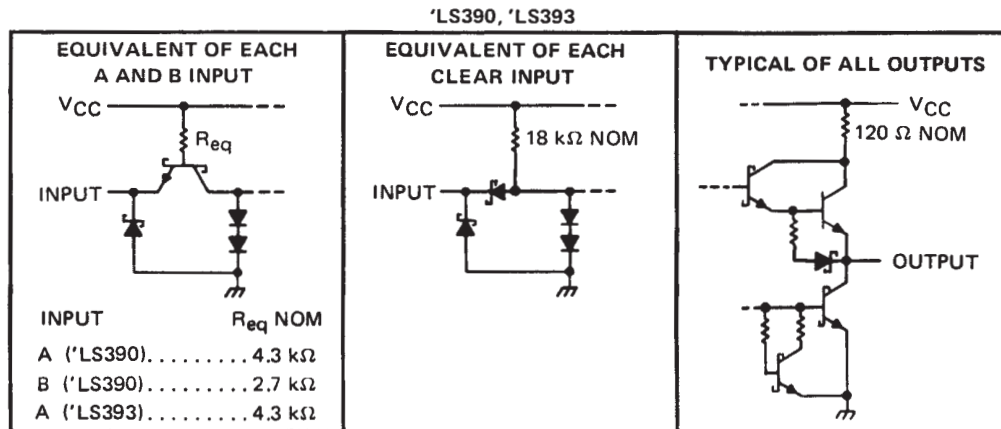
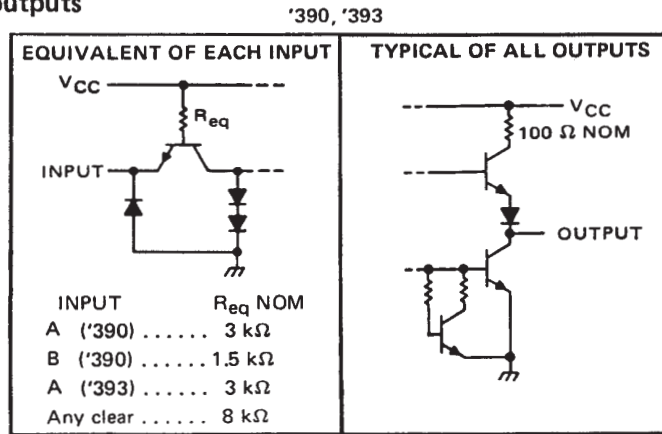
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logic diagrams (continued)



Pin numbers shown are for D, J, N and W packages.

schematics of inputs and outputs



# SN54390, SN54LS390, SN54393, SN54LS393 SN74390, SN74LS390, SN74393, SN74LS393 DUAL 4-BIT DECADE AND BINARY COUNTERS

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN54390, SN54393	-55°C to 125°C
SN74390, SN74393	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

## recommended operating conditions

	SN54390 SN54393			SN74390 SN74393			UNIT	
	MIN	NOM	MAX	MIN	NOM	MAX		
Supply voltage, $V_{CC}$	4.5	5	5.5	4.75	5	5.25	V	
High-level output current, $I_{OH}$	-800			-800			$\mu$ A	
Low-level output current, $I_{OL}$	16			16			mA	
Count frequency, $f_{count}$	A input		0	25	0		25	MHz
	B input		0	20	0		20	
Pulse width, $t_w$	A input high or low		20		20		ns	
	B input high or low		25		25			
	Clear high		20		20			
Clear inactive-state setup time, $t_{SU}$	25↓		25↓		25↓		ns	
Operating free-air temperature, $T_A$	-55		125		0		70	°C

↓ The arrow indicates that the falling edge of the clock pulse is used for reference.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	'390			'393			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
$V_{IH}$ High-level input voltage		2			2			V
$V_{IL}$ Low-level input voltage		0.8			0.8			V
$V_{IK}$ Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$	-1.5			-1.5			V
$V_{OH}$ High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -800 \mu\text{A}$	2.4	3.4		2.4	3.4		V
$V_{OL}$ Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 16 \text{ mA}¶$	0.2	0.4		0.2	0.4		V
$I_I$ Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$	1			1			mA
$I_{IH}$ High-level input current	Clear	40			40			$\mu$ A
	Input A	80			80			
	Input B	120						
$I_{IL}$ Low-level input current	Clear	-1			-1			mA
	Input A	-3.2			-3.2			
	Input B	-4.8						
$I_{OS}$ Short-circuit output current §	$V_{CC} = \text{MAX}$	SN54'	-20	-57	-20	-57	mA	
		SN74'	-18	-57	-18	-57		
$I_{CC}$ Supply current	$V_{CC} = \text{MAX}, \text{ See Note 2}$	42	69		38	64	mA	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ .

§ Not more than one output should be shorted at a time.

¶ The  $Q_A$  outputs of the '390 are tested at  $I_{OL} = 16 \text{ mA}$  plus the limit value for  $I_{IL}$  for the B input. This permits driving the B input while maintaining full fan-out capability.

NOTE 2:  $I_{CC}$  is measured with all outputs open, both clear inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.



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 SN74390, SN74LS390, SN74393, SN74LS393  
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switching characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

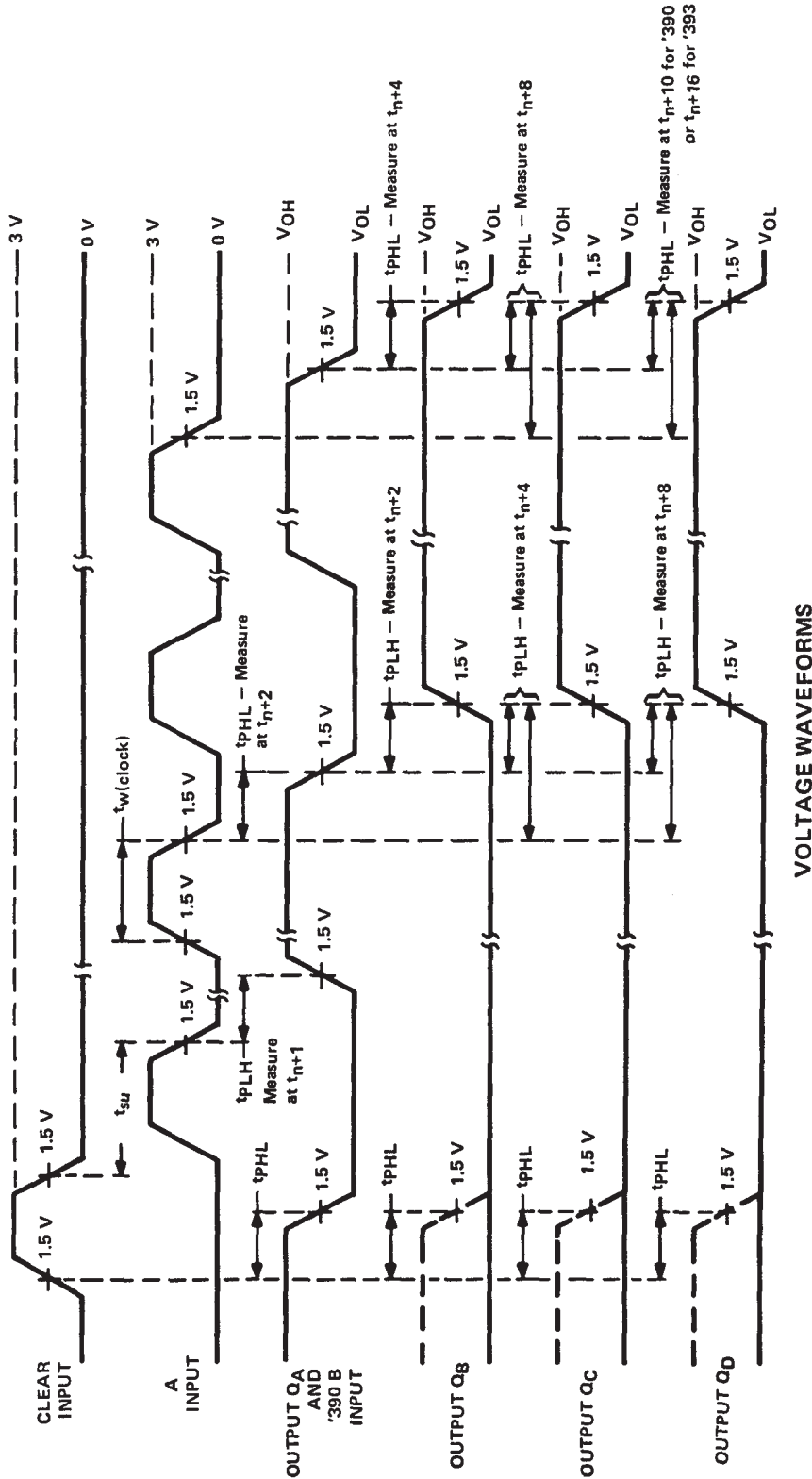
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'390			'393			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
$f_{\max}$	A	$Q_A$	$C_L = 15\text{ pF}$ , $R_L = 400\ \Omega$ , See Note 3 and Figure 1	25	35		25	35	MHz	
	B	$Q_B$		20	30					
$t_{PLH}$	A	$Q_A$		12	20		12	20	ns	
$t_{PHL}$				13	20		13	20		
$t_{PLH}$	A	$Q_C$ of '390 $Q_D$ of '393		37	60		40	60	ns	
$t_{PHL}$				39	60		40	60		
$t_{PLH}$	B	$Q_B$		13	21				ns	
$t_{PHL}$				14	21					
$t_{PLH}$	B	$Q_C$		24	39				ns	
$t_{PHL}$				26	39					
$t_{PLH}$	B	$Q_D$		13	21				ns	
$t_{PHL}$				14	21					
$t_{PHL}$	Clear	Any		24	39		24	39	ns	

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

SN54390, SN54LS390, SN54393, SN54LS393  
 SN74390, SN74LS390, SN74393, SN74LS393  
 DUAL 4-BIT DECADE AND BINARY COUNTERS

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PARAMETER MEASUREMENT INFORMATION



NOTE A: Input pulses are supplied by a generator having the following characteristics  $t_r \leq 5 \text{ ns}$ ,  $t_f \leq 5 \text{ ns}$ ,  $\text{PRR} = 1 \text{ MHz}$ , duty cycle = 50%,  $Z_{out} \approx 50 \text{ ohms}$ .

FIGURE 1

# SN54390, SN54LS390, SN54393, SN54LS393 SN74390, SN74LS390, SN74393, SN74LS393 DUAL 4-BIT DECADE AND BINARY COUNTERS

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Clear input voltage	7 V
Any A or B clock input voltage	5.5 V
Operating free-air temperature range: SN54LS390, SN54LS393	-55°C to 125°C
SN74LS390, SN74LS393	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

## recommended operating conditions

	SN54LS390 SN54LS393			SN74LS390 SN74LS393			UNIT	
	MIN	NOM	MAX	MIN	NOM	MAX		
Supply voltage, $V_{CC}$	4.5	5	5.5	4.75	5	5.25	V	
High-level output current, $I_{OH}$			-400			-400	$\mu$ A	
Low-level output current, $I_{OL}$			4			8	mA	
Count frequency, $f_{count}$	A input		0	25	0		25	MHz
	B input		0	12.5	0		12.5	
Pulse width, $t_w$	A input high or low		20		20		ns	
	B input high or low		40		40			
	Clear high		20		20			
Clear inactive-state setup time, $t_{SU}$	25 $\downarrow$		25 $\downarrow$				ns	
Operating free-air temperature, $T_A$	-55		125		0		70	°C

$\downarrow$  The arrow indicates that the falling edge of the clock pulse is used for reference.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS <sup>†</sup>	SN54LS'			SN74LS'			UNIT
		MIN	TYP <sup>‡</sup>	MAX	MIN	TYP <sup>‡</sup>	MAX	
$V_{IH}$ High-level input voltage		2			2			V
$V_{IL}$ Low-level input voltage		0.7			0.8			V
$V_{IK}$ Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$	-1.5			-1.5			V
$V_{OH}$ High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OH} = -400 \mu\text{A}$	2.5	3.4		2.7	3.4		V
$V_{OL}$ Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V},$	$I_{OL} = 4 \text{ mA}$ <sup>¶</sup>		0.25	0.4	0.25	0.4	V
		$I_{OL} = 8 \text{ mA}$ <sup>¶</sup>				0.35	0.5	
$I_I$ Input current at maximum input voltage	Clear	$V_{CC} = \text{MAX}$		$V_I = 7 \text{ V}$		0.1	0.1	mA
	Input A			$V_I = 5.5 \text{ V}$		0.2	0.2	
	Input B					0.4	0.4	
$I_{IH}$ High-level input current	Clear	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$				0.02	0.02	mA
	Input A					0.1	0.1	
	Input B					0.2	0.2	
$I_{IL}$ Low-level input current	Clear	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$				-0.4	-0.4	mA
	Input A					-1.6	-1.6	
	Input B					-2.4	-2.4	
$I_{OS}$ Short-circuit output current <sup>§</sup>	$V_{CC} = \text{MAX}$	-20	-100	-20	-100			mA
$I_{CC}$ Supply current	$V_{CC} = \text{MAX},$ See Note 2	'LS390		15	26	15	26	mA
		'LS393		15	26	15	26	

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>‡</sup> All typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ .

<sup>§</sup> Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

<sup>¶</sup> The  $Q_A$  outputs of the 'LS390 are tested at  $I_{OL} = \text{MAX}$  plus the limit value for  $I_{IL}$  for the clock B input. This permits driving the clock B input while maintaining full fan-out capability.

NOTE 2:  $I_{CC}$  is measured with all outputs open, both clear inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.



**SN54390, SN54LS390, SN54393, SN54LS393  
 SN74390, SN74LS390, SN74393, SN74LS393  
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switching characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

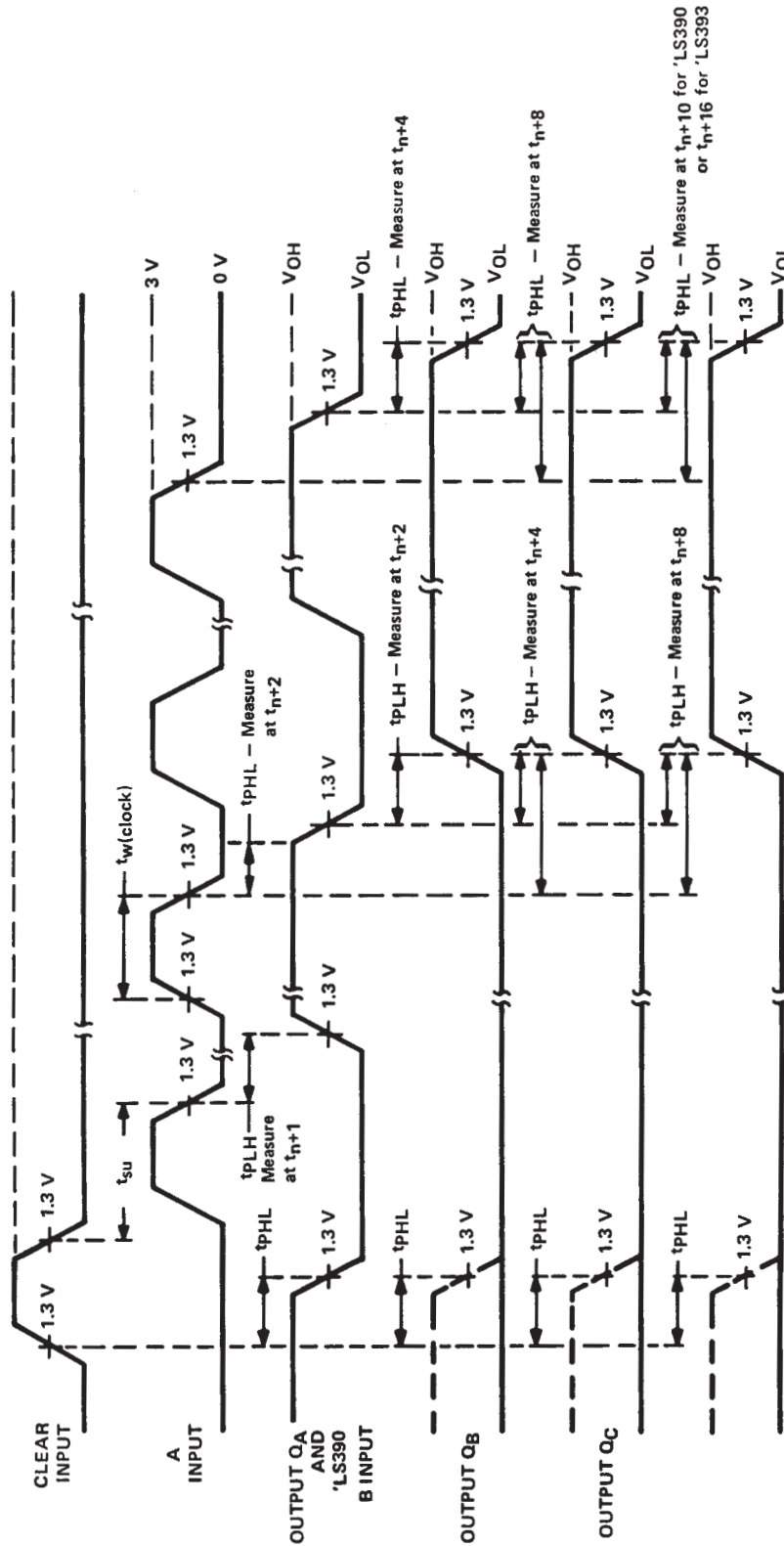
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS390			'LS393			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
$f_{\max}$	A	$Q_A$	$C_L = 15\text{ pF}$ , $R_L = 2\text{ k}\Omega$ , See Note 4 and Figure 2	25	35		25	35		MHz
	B	$Q_B$		12.5	20					
$t_{PLH}$	A	$Q_A$		12	20		12	20		ns
$t_{PHL}$				13	20		13	20		
$t_{PLH}$	A	$Q_C$ of 'LS390		37	60		40	60		ns
$t_{PHL}$		$Q_D$ of 'LS393		39	60		40	60		
$t_{PLH}$	B	$Q_B$		13	21					ns
$t_{PHL}$				14	21					
$t_{PLH}$	B	$Q_C$		24	39					ns
$t_{PHL}$				26	39					
$t_{PLH}$	B	$Q_D$		13	21					ns
$t_{PHL}$				14	21					
$t_{PHL}$	Clear	Any		24	39		24	39		ns

NOTE 4: Load circuits and voltage waveforms are shown in Section 1.





PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

NOTE A: Input pulses are supplied by a generator having the following characteristics  $t_r \leq 15$  ns,  $t_f \leq 6$  ns, PRR = 1 MHz, duty cycle = 50 %,  $Z_{out} \approx 50$  ohms.

FIGURE 2

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
7802601EA	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	Level-NC-NC-NC
7802601FA	ACTIVE	CFP	W	16	1	TBD	A42	Level-NC-NC-NC
7802601FA	ACTIVE	CFP	W	16	1	TBD	A42	Level-NC-NC-NC
JM38510/32701B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	Level-NC-NC-NC
JM38510/32701B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	Level-NC-NC-NC
JM38510/32701BEA	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	Level-NC-NC-NC
JM38510/32701BEA	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	Level-NC-NC-NC
JM38510/32702B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	Level-NC-NC-NC
JM38510/32702B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	Level-NC-NC-NC
JM38510/32702BCA	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	Level-NC-NC-NC
JM38510/32702BCA	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	Level-NC-NC-NC
JM38510/32702BDA	ACTIVE	CFP	W	14	1	TBD	A42	Level-NC-NC-NC
JM38510/32702BDA	ACTIVE	CFP	W	14	1	TBD	A42	Level-NC-NC-NC
JM38510/32702SCA	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	Level-NC-NC-NC
JM38510/32702SCA	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	Level-NC-NC-NC
JM38510/32702SDA	ACTIVE	CFP	W	14	1	TBD	A42	Level-NC-NC-NC
JM38510/32702SDA	ACTIVE	CFP	W	14	1	TBD	A42	Level-NC-NC-NC
SN54393J	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI
SN54393J	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI
SN54LS390J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	Level-NC-NC-NC
SN54LS390J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	Level-NC-NC-NC
SN54LS393J	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	Level-NC-NC-NC
SN54LS393J	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	Level-NC-NC-NC
SN74390N	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74390N	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74393N	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
SN74393N	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
SN74393N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
SN74393N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
SN74LS390D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS390D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS390DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS390DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS390DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS390DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS390DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS390DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
						no Sb/Br)		
SN74LS390N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74LS390N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74LS390N3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74LS390N3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74LS390NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS390NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS390NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS390NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS393D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS393D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS393DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS393DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS393DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS393DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS393DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS393DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS393J	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI
SN74LS393J	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI
SN74LS393N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74LS393N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74LS393N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
SN74LS393N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
SN74LS393NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74LS393NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74LS393NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS393NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS393NSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS393NSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
no Sb/Br)								
SNJ54393J	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI
SNJ54393J	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI
SNJ54393W	OBSOLETE	CFP	W	14		TBD	Call TI	Call TI
SNJ54393W	OBSOLETE	CFP	W	14		TBD	Call TI	Call TI
SNJ54LS390FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	Level-NC-NC-NC
SNJ54LS390FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	Level-NC-NC-NC
SNJ54LS390J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	Level-NC-NC-NC
SNJ54LS390J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	Level-NC-NC-NC
SNJ54LS390W	ACTIVE	CFP	W	16	1	TBD	A42	Level-NC-NC-NC
SNJ54LS390W	ACTIVE	CFP	W	16	1	TBD	A42	Level-NC-NC-NC
SNJ54LS393FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	Level-NC-NC-NC
SNJ54LS393FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	Level-NC-NC-NC
SNJ54LS393J	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	Level-NC-NC-NC
SNJ54LS393J	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	Level-NC-NC-NC
SNJ54LS393W	ACTIVE	CFP	W	14	1	TBD	A42	Level-NC-NC-NC
SNJ54LS393W	ACTIVE	CFP	W	14	1	TBD	A42	Level-NC-NC-NC

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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