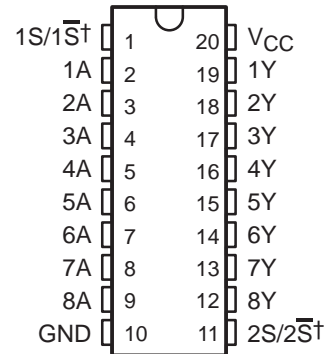


# SN75128, SN75129 EIGHT-CHANNEL LINE RECEIVERS

SLLS076B – JANUARY 1977 – REVISED MAY 1995

- Meets or Exceeds the Requirements of IBM™ System 360/370 Input/Output Specification
- Input Resistance . . . 7 kΩ to 20 kΩ
- Output Compatible With TTL
- Schottky-Clamped Transistors
- Operates From a Single 5-V Supply
- High Speed . . . Low Propagation Delay
- Ratio Specification . . .  $t_{PLH}/t_{PHL}$
- Common Strobe for Each Group of Four Receivers
- SN75128 . . . Active-High Strobes  
SN75129 . . . Active-Low Strobes

N PACKAGE  
(TOP VIEW)



† S and  $\bar{S}$  for SN75128 and SN75129, respectively

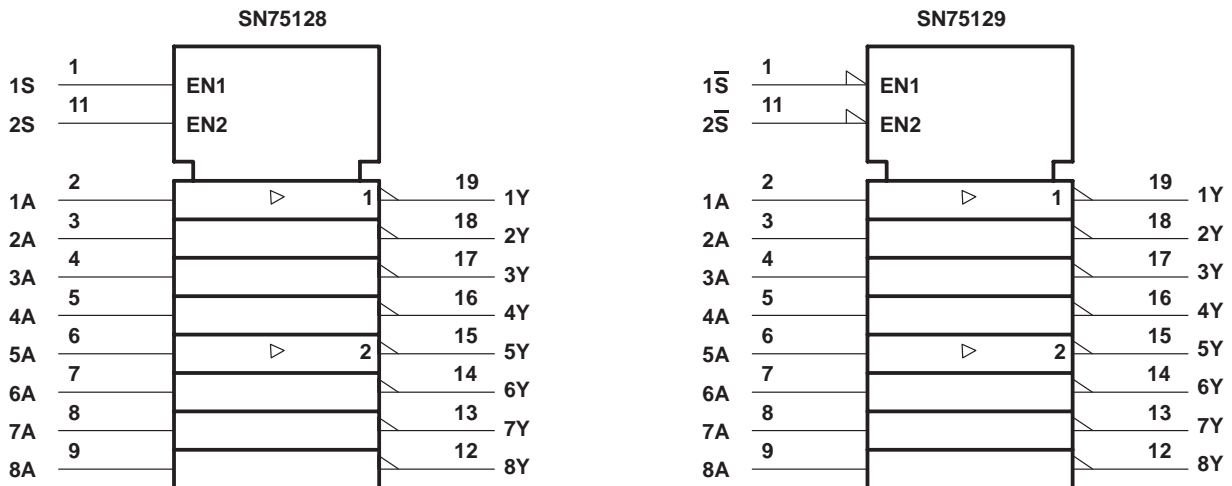
## description

The SN75128 and SN75129 are eight-channel line receivers designed to satisfy the requirements of the input-output interface specification for IBM 360/370. Both devices feature common strobes for each group of four devices. The SN75128 has active-high strobes; the SN75129 has active-low strobes. Special low-power design and Schottky-diode-clamped transistors allow low supply-current requirements while maintaining fast switching speeds and high-current TTL outputs.

For new IBM 360/370 interface designs, see the SN751730.

The SN75128 and SN75129 are characterized for operation from 0°C to 70°C.

## logic symbols†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

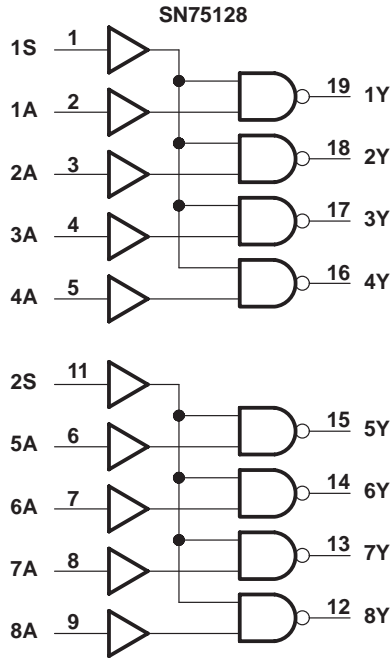
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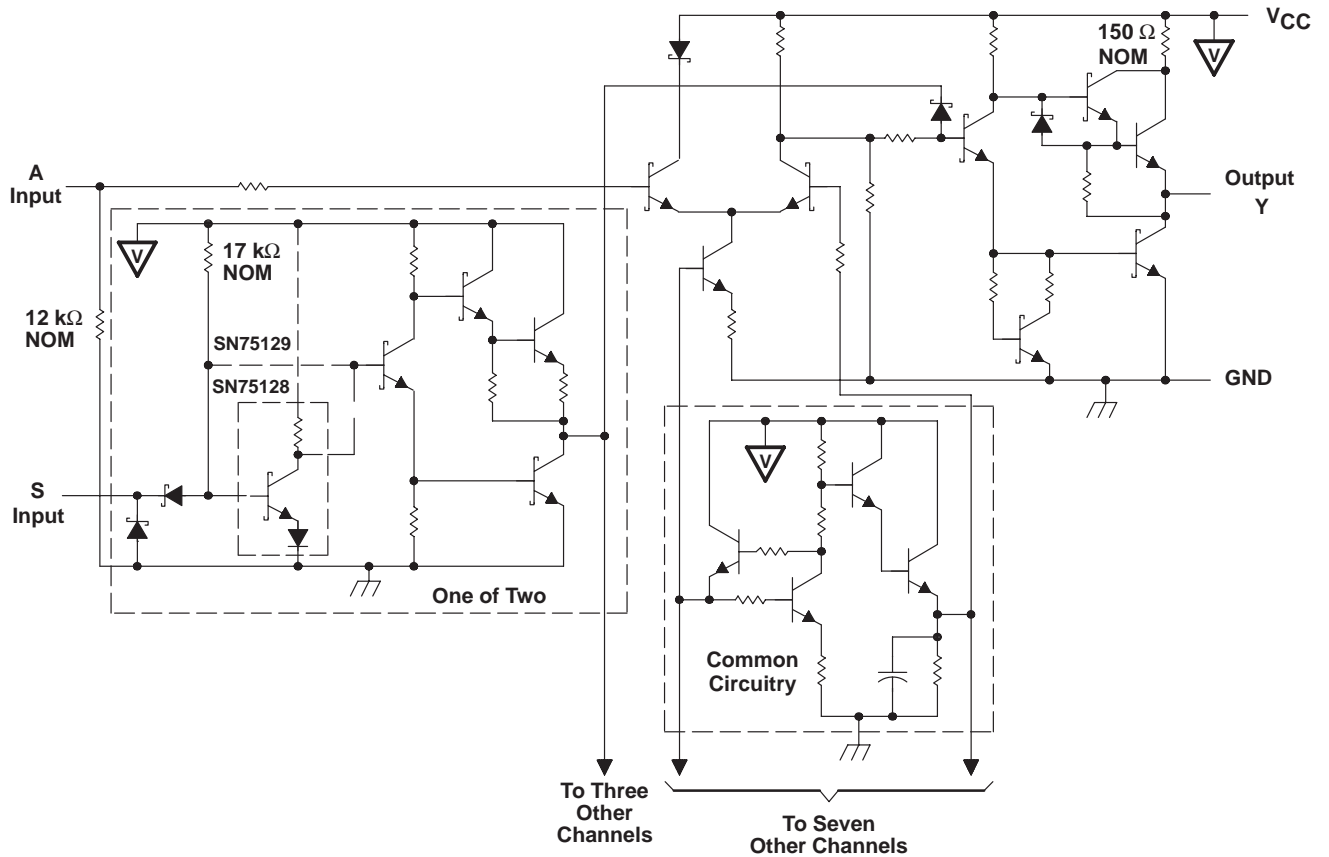
# SN75128, SN75129 EIGHT-CHANNEL LINE RECEIVERS

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## logic diagrams (positive logic)



## schematic (each driver)



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Input voltage range, $V_I$ (A)	-0.15 V to 7 V
Input voltage, $V_I$ (S)	7 V
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, $T_A$	0°C to 70°C
Storage temperature range, $T_{stg}$	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to network ground terminal.

**DISSIPATION RATING TABLE**

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING
N	1150 mW	9.2 mW/°C	736 mW

**recommended operating conditions**

	MIN	NOM	MAX	UNIT
Supply voltage, $V_{CC}$	4.5	5	5.5	V
High-level input voltage, $V_{IH}$	A	1.7		V
	S	2		
Low-level input voltage, $V_{IL}$	A		0.7	V
	S		0.7	
High-level output current, $I_{OH}$			-0.4	mA
Low-level output current, $I_{OL}$			16	mA
Operating free-air temperature, $T_A$	0		70	°C

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$V_{OH}$ High-level output voltage	$V_{CC} = 4.5\text{ V}$ , $V_{IL} = 0.7\text{ V}$ , $I_{OH} = -0.4\text{ mA}$	2.4	3.1		V
$V_{OL}$ Low-level output voltage	$V_{CC} = 4.5\text{ V}$ , $V_{IH} = 1.7\text{ V}$ , $I_{OL} = 16\text{ mA}$		0.4	0.5	V
$V_{IK}$ Input clamp voltage	S $V_{CC} = 4.5\text{ V}$ , $I_I = -18\text{ mA}$			-1.5	V
$I_{IH}$ High-level input current	A $V_{CC} = 5.5\text{ V}$ , $V_I = 3.11\text{ V}$		0.3	0.42	mA
	S $V_{CC} = 5.5\text{ V}$ , $V_I = 2.7\text{ V}$			20	μA
$I_{IL}$ Low-level input current	A $V_{CC} = 5.5\text{ V}$ , $V_I = 0.15\text{ V}$			30	μA
	S $V_{CC} = 5.5\text{ V}$ , $V_I = 0.4\text{ V}$			-0.4	mA
$I_{OS}$ Short-circuit output current‡	$V_{CC} = 5.5\text{ V}$ , $V_O = 0$	-18		-60	mA
$r_I$ Input resistance	$V_{CC} = 4.5\text{ V}$ , 0 V or open, $\Delta V_I = 0.15\text{ V to } 4.15\text{ V}$	7		20	kΩ
$I_{CC}$ Supply current	SN75128 $V_{CC} = 5.5\text{ V}$ , Strobe at 2.4 V, All A inputs at 0.7 V		19	31	mA
	SN75129 $V_{CC} = 5.5\text{ V}$ , Strobe at 0.4 V, All A inputs at 0.7 V		19	31	
	SN75128 $V_{CC} = 5.5\text{ V}$ , Strobe at 2.4 V, All A inputs at 4 V		32	53	
	SN75129 $V_{CC} = 5.5\text{ V}$ , Strobe at 0.4 V, All A inputs at 4 V		32	53	

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ Not more than one output should be shorted at a time.

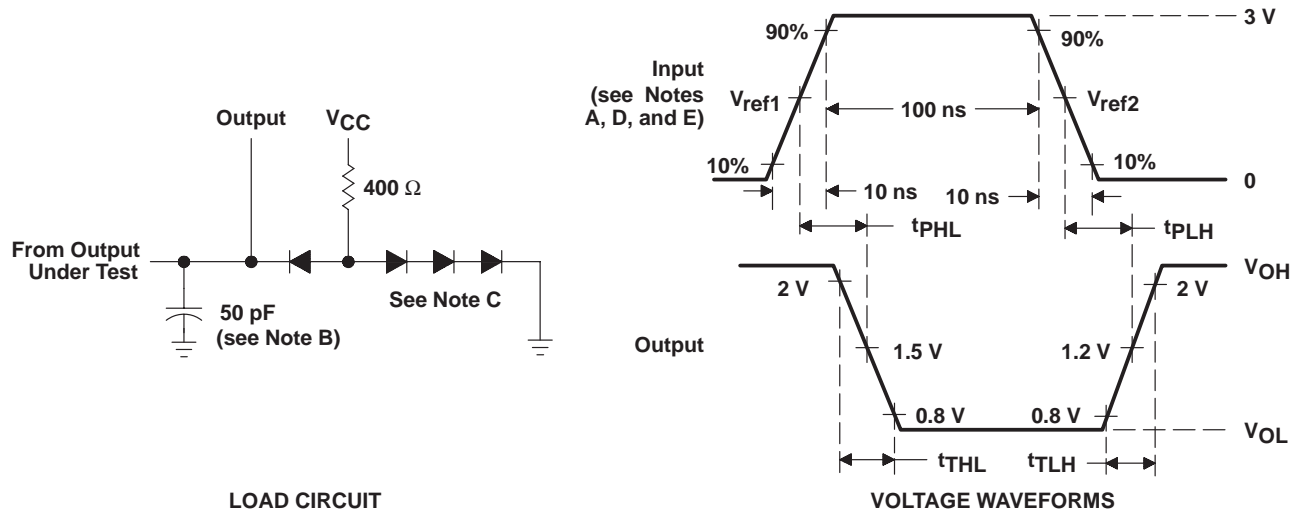
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switching characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	FROM	TEST CONDITIONS	SN75128			SN75129			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$t_{PLH}$ Propagation delay time, low-to-high-level output	A	$R_L = 400\ \Omega$ , $C_L = 50\ \text{pF}$ , See Figure 1	7	14	25	7	14	25	ns
$t_{PHL}$ Propagation delay time, high-to-low-level output			10	18	30	10	18	30	ns
$t_{PLH}$ Propagation delay time, low-to-high-level output	S		26	40		20	35	ns	
$t_{PHL}$ Propagation delay time, high-to-low-level output			22	35		16	30	ns	
$\frac{t_{PLH}}{t_{PHL}}$ Ratio of propagation delay times	A		0.5	0.8	1.3	0.5	0.8	1.3	
$t_{TLH}$ Transition time, low-to-high-level output			1	7	12	1	7	12	ns
$t_{THL}$ Transition time, high-to-low-level output		1	3	12	1	3	12	ns	

## PARAMETER MEASUREMENT INFORMATION



- NOTES: A. Input pulses are supplied by a generator having the following characteristics:  $Z_O = 50\ \Omega$ ,  $PRR \leq 5\ \text{MHz}$ .  
 B. Includes probe and jig capacitance  
 C. All diodes are 1N3064 or equivalent.  
 D. The strobe inputs of SN75129 are in phase with the output.  
 E.  $V_{ref1} = 0.7\ \text{V}$  and  $V_{ref2} = 1.7\ \text{V}$  for testing data (A) inputs,  $V_{ref1} = V_{ref2} = 1.3\ \text{V}$  for strobe inputs.

Figure 1. Load Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

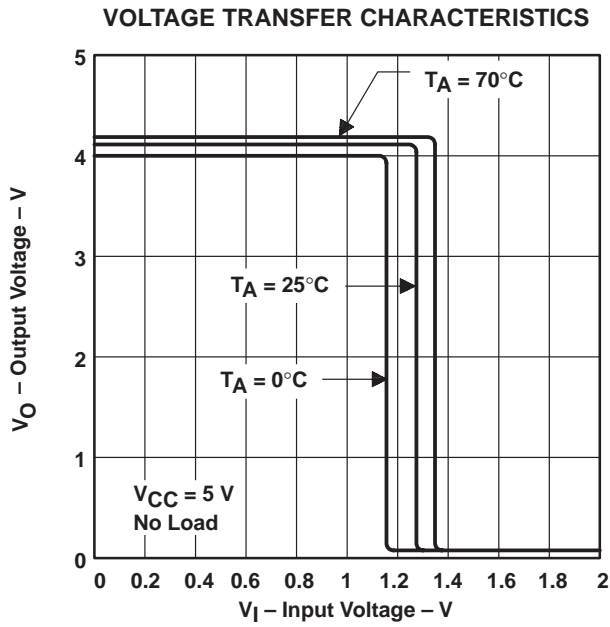


Figure 2

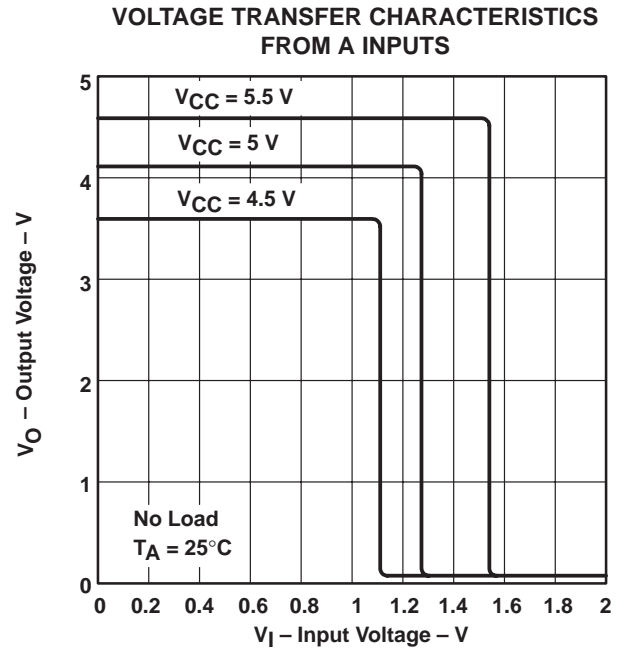


Figure 3

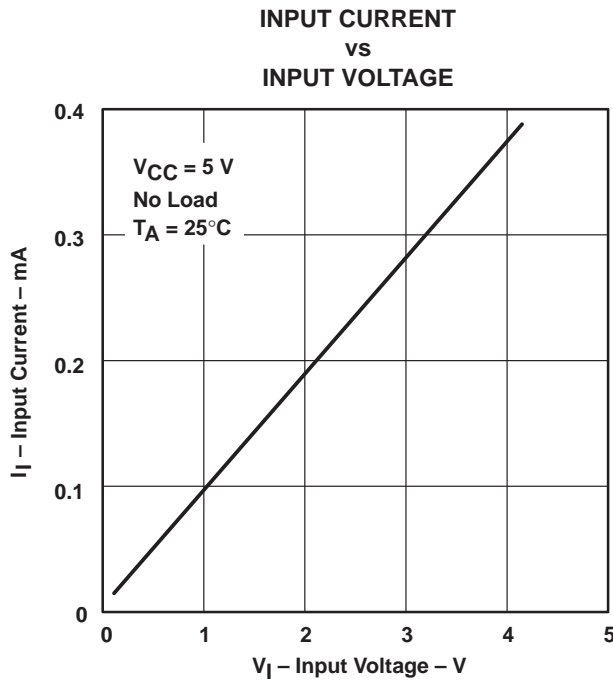


Figure 4

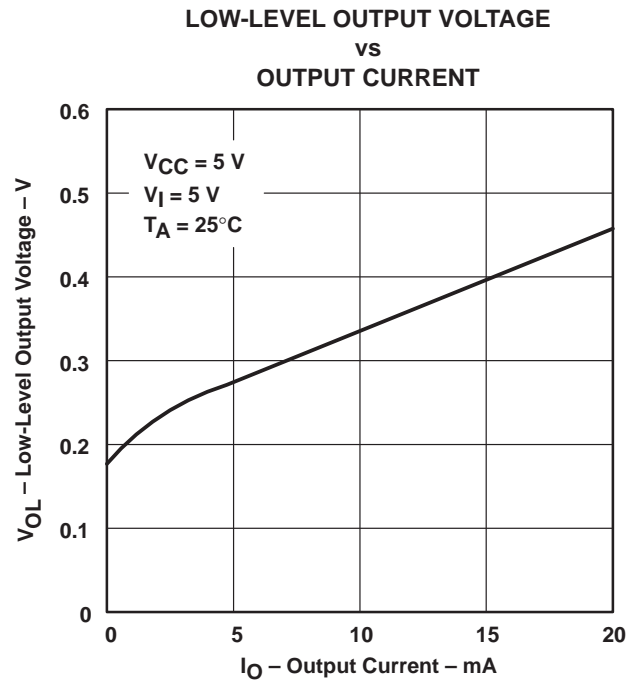


Figure 5



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