PLESSEY
Semiconductors

SP8719AC

520MHz ÷ 80/81 TWO MODULUS DIVIDER

(CONFORMS TO MIL-STD-883C CLASS B)

The SP8719 ÷80/81 is a 50mW programmable divider with a maximum specified operating frequency of 520MHz over the temperature range -55° C to +125° C.

The signal (clock) inputs are biased internally and require to be capacitor coupled. The output stage is of an unusual low power design featuring dynamic pull-up, and optimised for driving CMOS. The 0 to 1 output edge should be used to give the maximum loop delay.

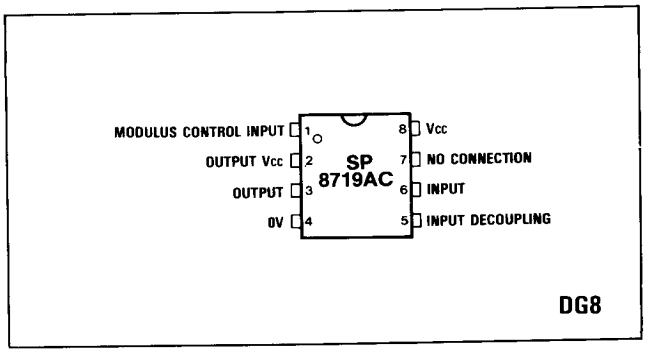


Fig.1 Pin connections - top view

FEATURES

- MIL-M-38510 Change Notification Observed
- Full Quality Conformance Inspection
- DC to 520MHz Operation
- Power Consumption: 55mW Typical
- Temperature Range: -55°C to +125°C
- Control Inputs and Outputs are CMOS Compatible

ABSOLUTE MAXIMUM RATINGS

Supply voltage (Pin 2 or 8):	8V
Storage temperature range:	-40° C to +150° C
Max. junction temperature:	+175° C
Max. clock I/P voltage:	2.5V p-p

CHANGE NOTIFICATION

The change notification requirements of MIL-M-38510 will be implemented on this device type. Known customers will be notified of any changes since last buy when ordering further parts if significant changes have been made.

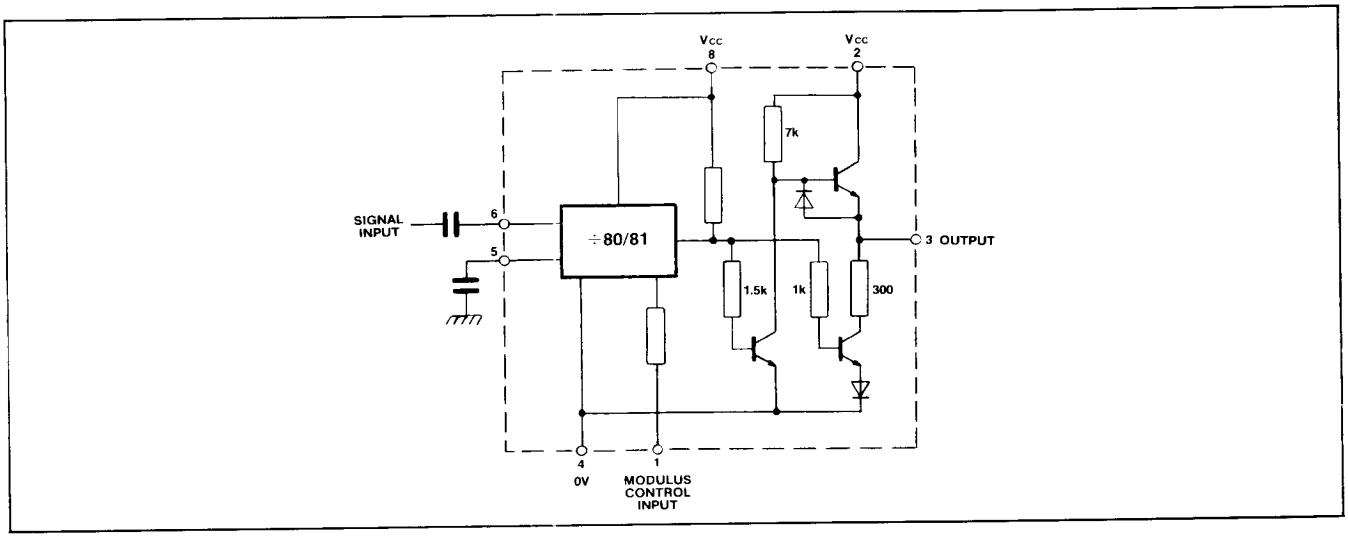


Fig.2 Functional diagram SP8719

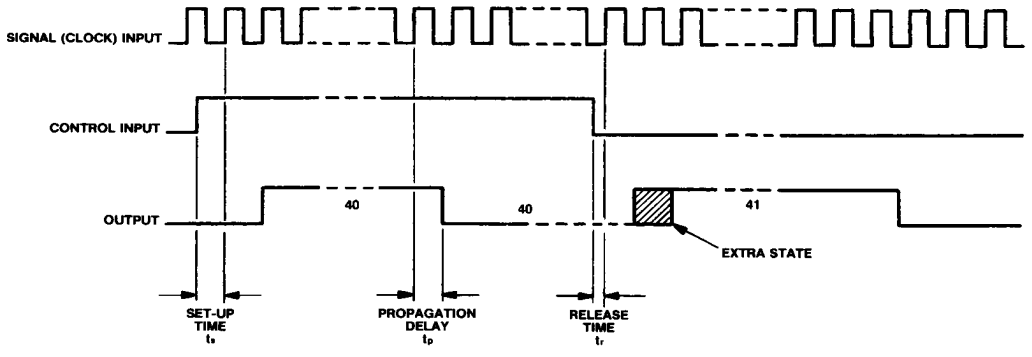
Rev.	A	B	
Date	2 Oct 86	11 Feb 87	

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage: V_{CC} = +4.95V to 5.45V, Temperature: T_{amb} = -55°C to +125°C

Parameter	Symbol	Value		Sub group	Notes	Method/Conditions/Temp.
		Min.	Max.			
Max. frequency	f_{max}	520MHz		9,10,11	Note 1	Input 125mV to 350mV p-p
Min. frequency (sinewave input)	f_{min}	-	30MHz	9,10,11	Note 1	Input 400mV to 800mV p-p
Function test		-	-	7,8	Note 2	
Power supply current	I_{CC}	-	11.9mA	1,2,3	-	C_L = 3pF; Pins 2,8 linked
Output high voltage	V_{OH}	(V_{CC} -1.2)		1,2,3	-	I_L = -0.2mA
Output low voltage	V_{OL}		1.2V	1,2,3	-	I_L = 0.2mA
Control input high voltage	V_{INH}	3.3V	8V	1,2,3	-	÷80
Control input low voltage	V_{INL}	0V	1.7V	1,2,3	-	÷81
Control input high current	I_{INH}		0.41mA	1,2,3	-	V_{INH} = 8V
Control input low current	I_{INL}	-0.20mA		1,2,3	-	V_{INL} = 0V

NOTES
1. The test configuration for dynamic testing is shown in Fig.5. Guaranteed operating window shown in Fig.4.
2. This test is carried out in conjunction with static tests (sub groups 1, 2 or 3) and is sufficient to verify the truth table defined in Fig.3.
3. Sub groups 4, 5 and 6 are not required.

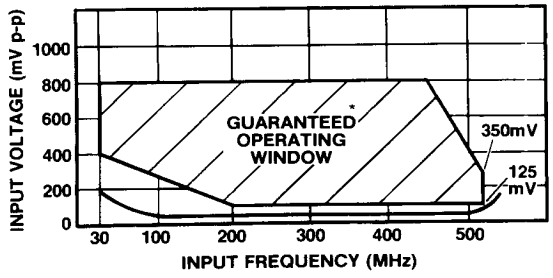


TRUTH TABLE

Control inputs	Division ratio
0	81
1	80

Fig.3 Timing diagram SP8719

NOTES
The set-up time t_s is defined as minimum time that can elapse between L→H transition of control input and the next L→H clock pulse transition to ensure that the ÷80 mode is obtained.
The release time t_r is defined as the minimum time that can elapse between a H→L transition of control input and the next L→H clock pulse transition to ensure that the ÷81 mode is obtained.



*Tested as specified in table of Electrical Characteristics

Fig.4 Input sensitivity

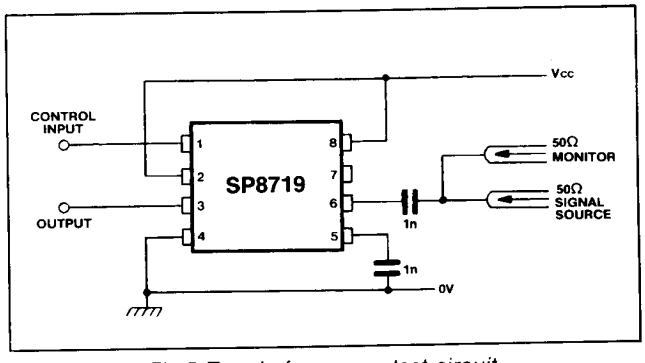


Fig.5 Toggle frequency test circuit

OPERATING NOTES

1. The inputs are biased internally and coupled to a signal source with suitable capacitors.
2. If no signal is present the device will self-oscillate. If this is undesirable it may be prevented by connecting a 15k resistor from one input to Pin 4 (ground). This will reduce the sensitivity.
3. The circuit will operate down to DC but slew rate must be better than 100V/μs.
4. The output stage is of an unusual design and is intended to interface with CMOS. External pull-up resistors or circuits must not be used.
5. This device is *NOT* suitable for driving TTL or its derivatives.

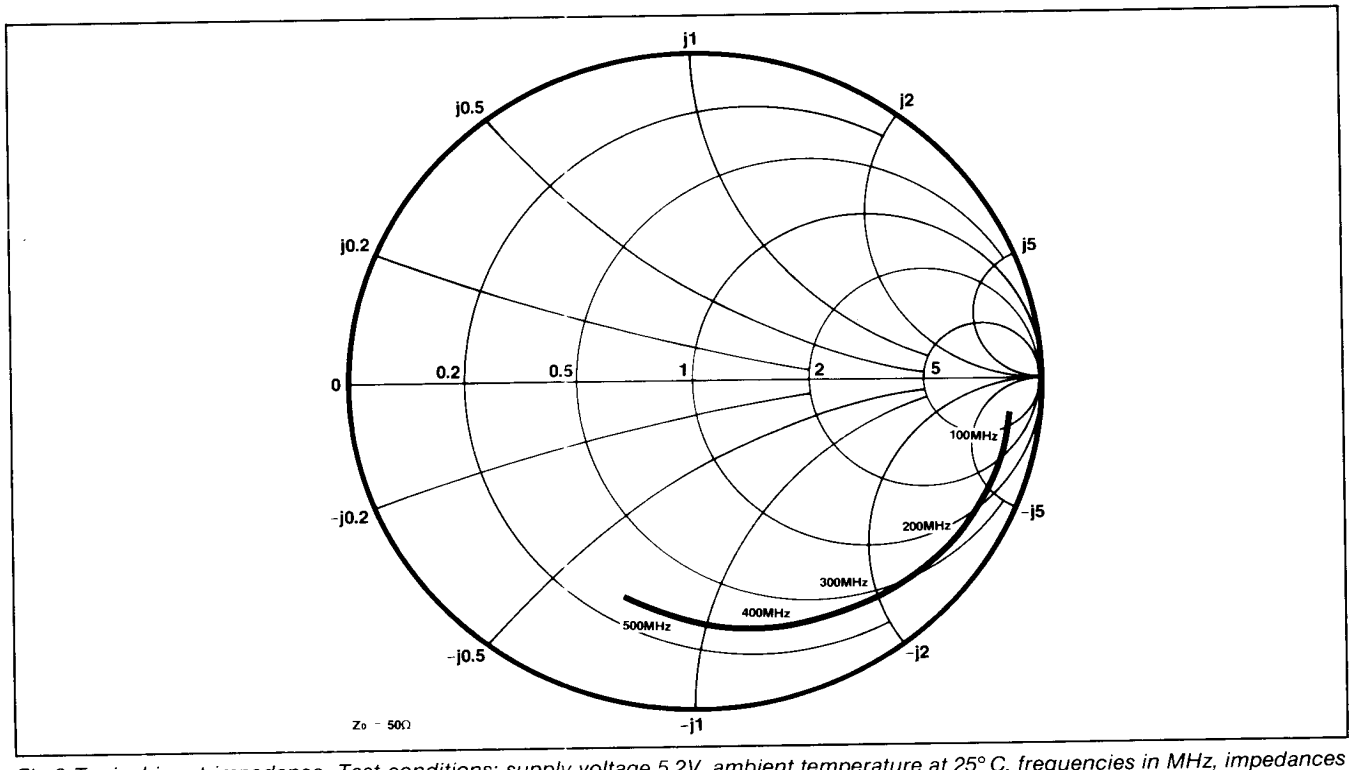


Fig.6 Typical input impedance. Test conditions: supply voltage 5.2V, ambient temperature at 25° C, frequencies in MHz, impedances normalised to 50 ohms.

GUARANTEED CHARACTERISTICS

The following characteristics are guaranteed for the SP8719AC at +25° C and over the full supply voltage range (-4.95V to -5.45V), but are not tested.

Parameter	Symbol	Value Min.	Value Max.	Test conditions
Clock to output delay	t_p	-	28ns	C_L = 10pF
Set-up time	t_s	10ns	-	C_L = 10pF
Release time	t_r	10ns	-	C_L = 10pF

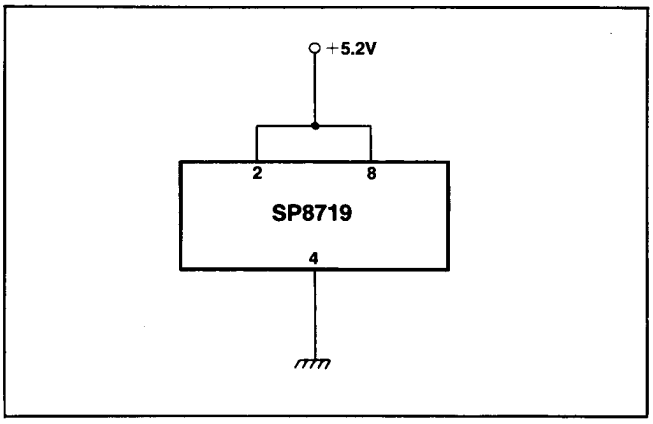


Fig.7 Burn-in/Life test circuit
NOTES (1) The device self-oscillates under above test condition
(2) PDA is 5% and based on sub groups 1 and 7