

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74ACT245P, TC74ACT245F, TC74ACT245FW, TC74ACT245FT
TC74ACT640P, TC74ACT640F, TC74ACT640FW, TC74ACT640FT

OCTAL BUS TRANSCEIVER
 TC74ACT245P/F/FW/FT 3-STATE, NON-INVERTING
 TC74ACT640P/F/FW/FT 3-STATE, INVERTING

(Note) The JEDEC SOP (FW) is not available in Japan.

The TC74ACT245 and 640 are advanced high speed CMOS OCTAL BUS TRANSCEIVERS fabricated with silicon gate and double-layer metal wiring C²MOS technology. They achieve the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

These devices may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.

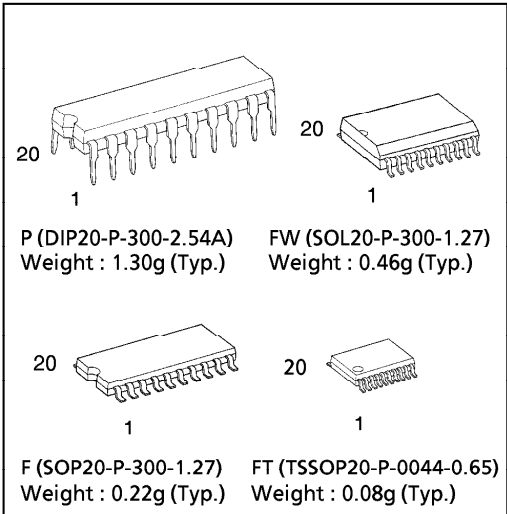
They are intended for two-way asynchronous communication between data busses. The direction of data transmission is determined by the level of the DIR input.

The enable input (\bar{G}) can be used to disable the device so that the busses are effectively isolated.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES :

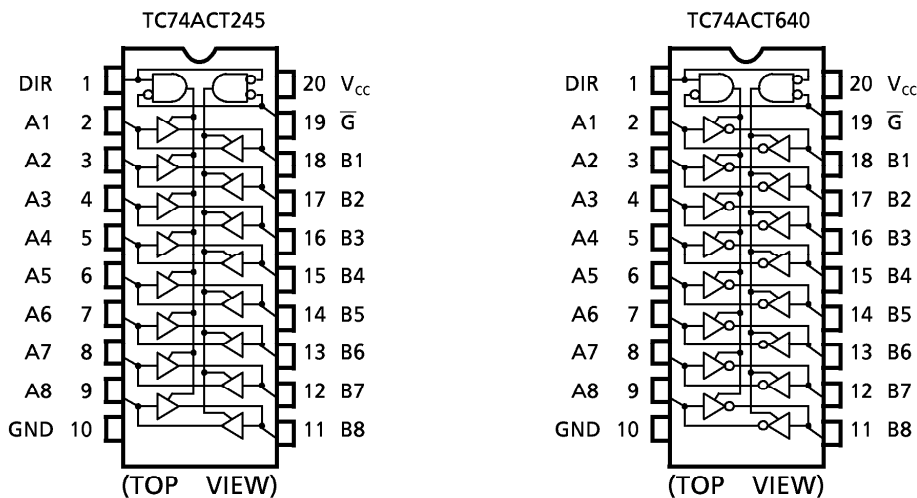
- High Speed..... $t_{pd} = 4.7ns(\text{typ.})$ at $V_{CC} = 5V$
- Low Power Dissipation..... $I_{CC} = 8\mu A(\text{Max.})$ at $T_a = 25^\circ C$
- Compatible with TTL outputs... $V_{IL} = 0.8V(\text{Max.})$
 $V_{IH} = 2.0V(\text{Min.})$
- Symmetrical Output Impedance... $|I_{OH}| = |I_{OL}| = 24mA(\text{Min.})$
 Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays..... $t_{pLH} \approx t_{pHL}$
- Pin and Function Compatible with 74F245/640



APPLICATION NOTES

- 1) Do not apply a signal to any bus terminal when it is in the out put mode. Damage may result.
- 2) All floating (high impedance) bus terminals must have their input levels fixed by means of pull up or pull down resistors.

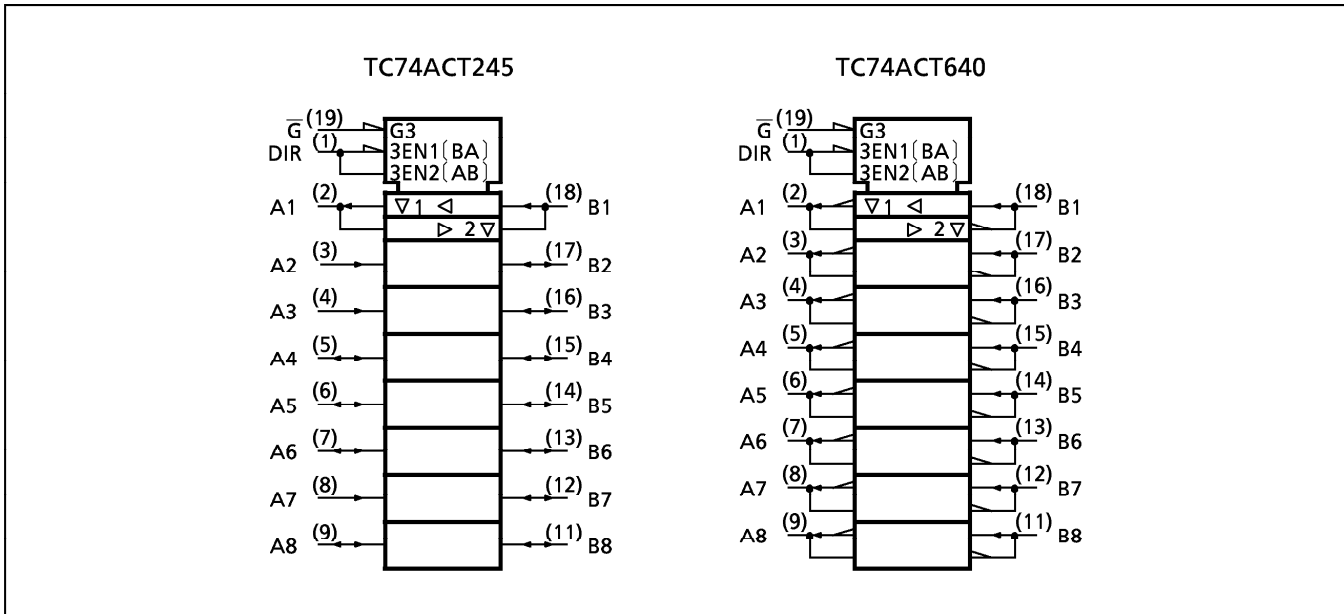
PIN ASSIGNMENT



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IEC LOGIC SYMBOL



TRUTH TABLE

INPUTS		FUNCTION		OUTPUTS	
\bar{G}	DIR	A BUS	B BUS	ACT245	ACT640
L	L	OUTPUT	INPUT	A = B	A = \bar{B}
L	H	INPUT	OUTPUT	B = A	B = \bar{A}
H	X	High Impedance		Z	Z

X : Don't Care
Z : High Impedance

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ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5~7.0	V
DC Input Voltage	V_{IN}	-0.5~ $V_{CC} + 0.5$	V
DC Output Voltage	V_{OUT}	-0.5~ $V_{CC} + 0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 50	mA
DC Output Current	I_{OUT}	± 50	mA
DC V_{CC} /Ground Current	I_{CC}	± 200	mA
Power Dissipation	P_D	500 (DIP)* / 180 (SOP/TSSOP)	mW
Storage Temperature	T_{stg}	-65~150	°C

*500mW in the range of $T_a = -40^{\circ}\text{C} \sim 65^{\circ}\text{C}$. From $T_a = 65^{\circ}\text{C}$ to 85°C a derating factor of $-10\text{mW}/^{\circ}\text{C}$ should be applied up to 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5~5.5	V
Input Voltage	V_{IN}	0~ V_{CC}	V
Output Voltage	V_{OUT}	0~ V_{CC}	V
Operating Temperature	T_{opr}	-40~85	°C
Input Rise and Fall Time	dt/dV	0~10	ns/V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	$T_a = 25^{\circ}\text{C}$			$T_a = -40 \sim 85^{\circ}\text{C}$		UNIT	
				MIN.	TYP.	MAX.	MIN.	MAX.		
High - Level Input Voltage	V_{IH}		4.5 § 5.5	2.0	—	—	2.0	—	V	
Low - Level Input Voltage	V_{IL}		4.5 § 5.5	—	—	0.8	—	0.8	V	
High - Level Output Voltage	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -50\mu\text{A}$	4.5	4.4	4.5	—	4.4	—	V
			$I_{OH} = -24\text{mA}$	4.5	3.94	—	—	3.80	—	
			$I_{OH} = -75\text{mA}^*$	5.5	—	—	—	3.85	—	
Low - Level Output Voltage	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 50\mu\text{A}$	4.5	—	0.0	0.1	—	0.1	V
			$I_{OL} = 24\text{mA}$	4.5	—	—	0.36	—	0.44	
			$I_{OL} = 75\text{mA}^*$	5.5	—	—	—	—	1.65	
3 - State Output Off - State Current	I_{OZ}	$V_{IN} = V_{IH}$ or V_{IL} $V_{OUT} = V_{CC}$ or GND	5.5	—	—	± 0.5	—	± 5.0	μA	
Input Leakage Current	I_{IN}	$V_{IN} = V_{CC}$ or GND	5.5	—	—	± 0.1	—	± 1.0		
Quiescent Supply Current	I_{CC}	$V_{IN} = V_{CC}$ or GND	5.5	—	—	8.0	—	80.0		
Quiescent Supply Current	I_C	PER INPUT : $V_{IN} = 3.4\text{V}$ OTHER INPUT : V_{CC} or GND	5.5	—	—	1.35	—	1.5	mA	

* : This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

AC ELECTRICAL CHARACTERISTICS ($C_L = 50\text{pF}$, $R_L = 500\Omega$, Input $t_r = t_f = 3\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C			Ta = -40~85°C		UNIT	
			V _{CC} (V)	MIN.	TYP.	MAX.	MIN.		MAX.
Propagation Delay Time*	t_{pLH} t_{pHL}		5.0 ± 0.5	—	5.0	8.0	1.0	9.0	ns
Propagation Delay Time**	t_{pLH} t_{pHL}		5.0 ± 0.5	—	5.7	8.5	1.0	9.5	
Output Enable Time	t_{pZL} t_{pZH}		5.0 ± 0.5	—	7.3	12.3	1.0	14.0	
Output Disable Time	t_{pLZ} t_{pHZ}		5.0 ± 0.5	—	6.3	9.7	1.0	11.0	
Input Capacitance	C _{IN}	DIR, \bar{G}	—	—	5	10	—	10	pF
Bus Input Capacitance	C _{I/O}	An, Bn	—	—	13	—	—	—	
Power Dissipation Capacitance	C _{PD} (1)	TC74ACT245	—	—	38	—	—	—	
		TC74ACT640	—	—	43	—	—	—	

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

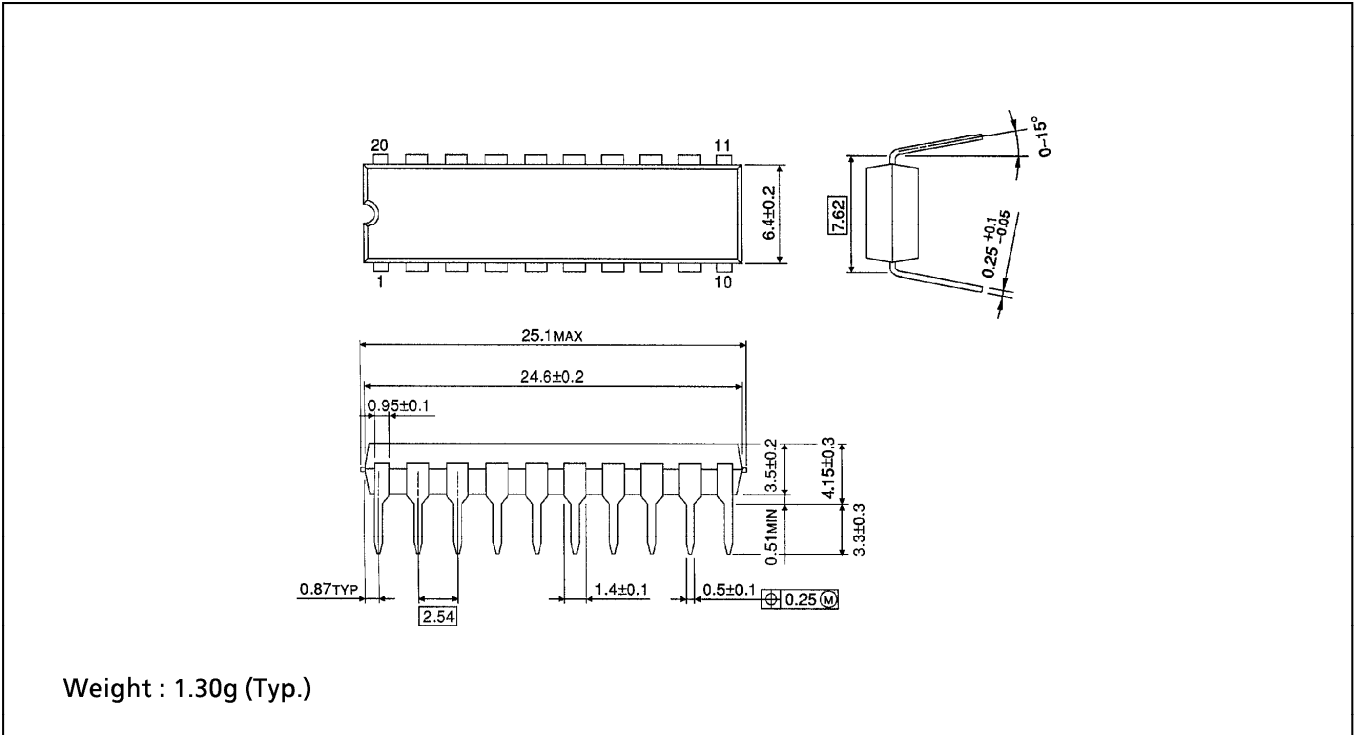
$$I_{CC}(\text{opr.}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per bit)}$$

(2) * for TC74ACT245 only

** for TC74ACT640 only

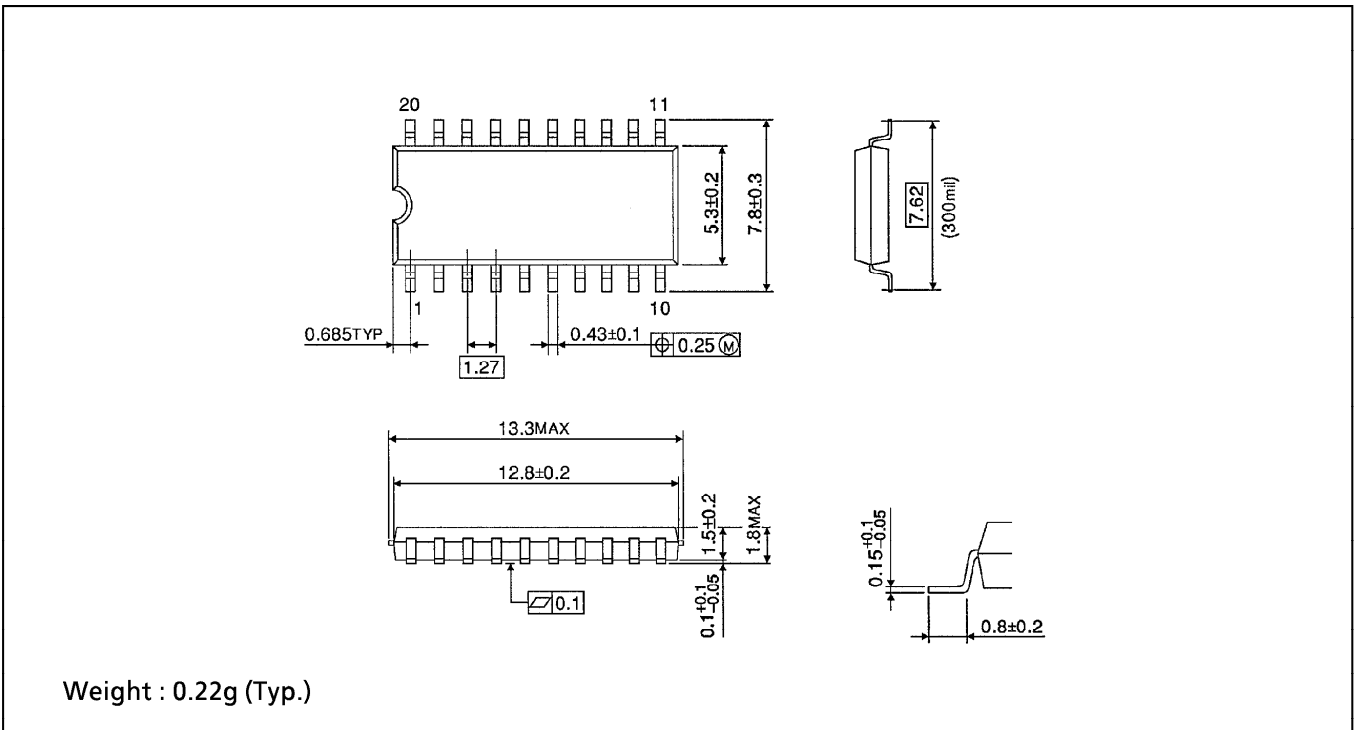
DIP 20PIN OUTLINE DRAWING (DIP20-P-300-2.54A)

Unit in mm



SOP 20PIN (200mil BODY) OUTLINE DRAWING (SOP20-P-300-1.27)

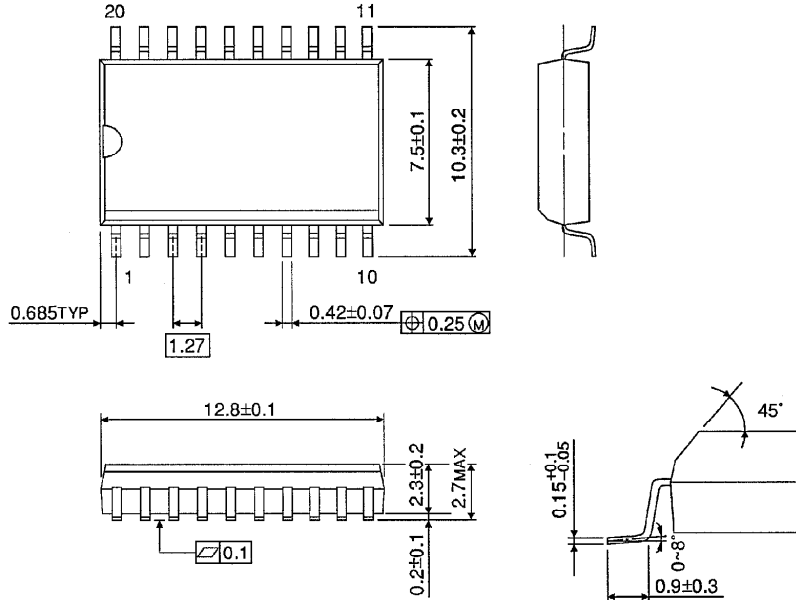
Unit in mm



SOP 20PIN (300mil BODY) OUTLINE DRAWING (SOL20-P-300-1.27)

Unit in mm

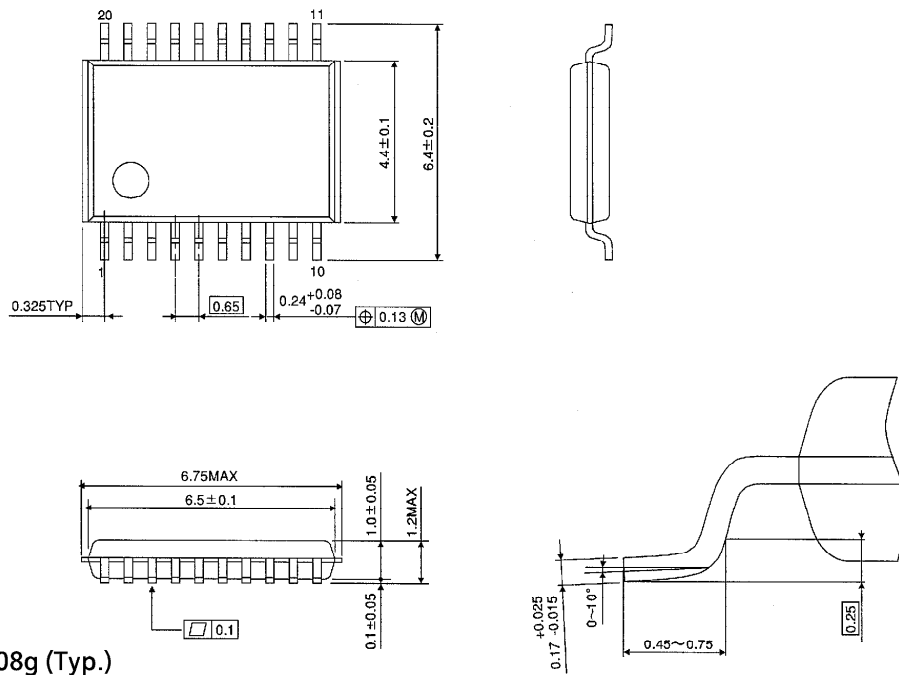
(Note) This package is not available in Japan.



Weight : 0.46g (Typ.)

TSSOP 20PIN OUTLINE DRAWING (TSSOP20-P-0044-0.65)

Unit in mm



Weight : 0.08g (Typ.)