TDA9210

150 MHz PIXEL VIDEO CONTROLLER FOR MONITORS

PRELIMINARY DATA

FEATURE

- 150 MHZ PIXEL RATE
- 2.7 ns RISE AND FALL TIME
- I^2C BUS CONTROLLED
- GREY SCALE TRACKING VERSUS BRIGHTNESS
- OSD MIXING
- NEGATIVE FEED-BACK FOR DC COUPLING APPLICATION
- BEAM CURRENT ATTENUATION (ABL)
- PEDESTRAL CLAMPING ON OUTPUT STAGE
- POSSIBILITY OF LIGHT OR DARK GREY OSD BACKGROUND
- OSD INDEPENDENT CONTRAST CONTROL
- ADJUSTABLE BANDWIDTH
- INPUT BLACK LEVEL CLAMPING WITH BUILT-IN CLAMPING PULSE
- STAND-BY MODE
- 5 V TO 8 V POWER SUPPLY
- SYNC CLIPPING FUNCTION (SOG)

DESCRIPTION

The TDA9210 is an I^2C Bus controlled RGB preamplifier designed for Monitor applications, able to mix the RGB signals coming from any OSD device. The usual Contrast, Brightness, Drive and Cut-Off Controls are provided.

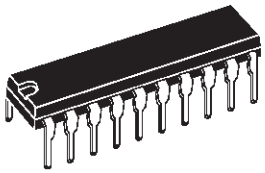
In addition, it includes the following features:

– OSD contrast,

– Bandwidth adjustment,

– Grey background,

– Internal back porch clamping pulse generator.



DIP20
(Plastic Package)

ORDER CODE: TDA9210

The RGB incoming signals are amplified and shaped to drive any commonly used video amplifiers without intermediate follower stages. Even though encapsulated in a 24-pin package only, this IC allows any kind of CRT Cathode coupling :

– AC coupling with DC restore,

– DC coupling with Feed-back from Cathodes,

– DC coupling with Cut-Off controls of the Video amplifier (ST Amplifiers TDA9533/9530).

As for any ST Video pre-amplifier, the TDA9210 is able to drive a real load without any external interface.

One of the main advantages of ST devices is their ability to sink and source currents while most of the devices from our competitors have problems to sink large currents.

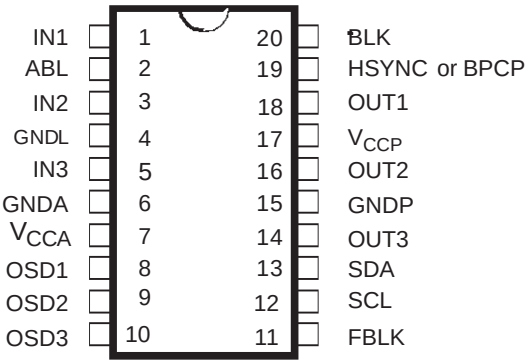
These driving capabilities combined with an original output stage structure suppress any static current on the output pins and therefore reduce dramatically the power dissipation of the device.

Extensive integration combined with high performance and advanced features make the TDA9210 one of the best choice for any CRT Monitor in the 14” to 17” range.

Perfectly matched with the ST Video Amplifiers TDA9535/36, these 2 products offer a complete solution for high performance and cost-optimized Video Board Application.

Version 3.1

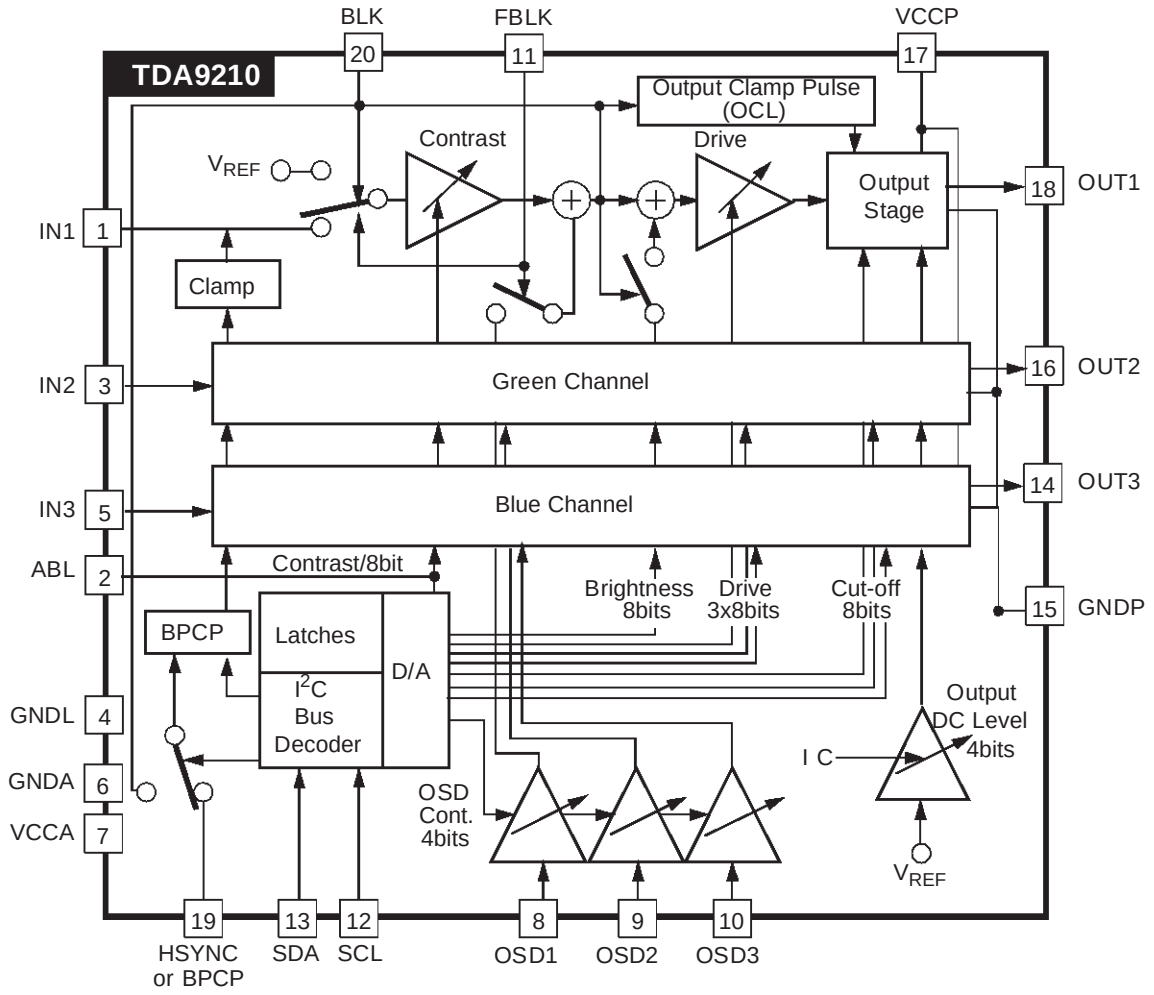
1 - PIN CONNECTIONS



2 - PIN DESCRIPTION

Pin Number	Symbol	Description
1	IN1	Red Video Input
2	ABL	ABL Input
3	IN2	Green Video Input
4	GNDL	Logic Ground
5	IN3	Blue Video Input
6	GNDA	Analog Ground
7	V_{CCA}	Analog V_{CC} (5V)
8	OSD1	Red OSD Input
9	OSD2	Green OSD Input
10	OSD3	Blue OSD Input
11	FBLK	Fast Blanking
12	SCL	SCL
13	SDA	SDA
14	OUT3	Blue Video Output
15	GNDP	Power Ground
16	OUT2	Green Video Output
17	V_{CCP}	Power V_{CC} (5 V to 8 V)
18	OUT1	Red Video Output
19	HSYNC/BPCP	HSYNC/BPCP
20	BLK	Blanking Input

3 - BLOCK DIAGRAM



See Figure 8 for complete BPCP and OCL generation diagram

4 - FUNCTIONAL DESCRIPTION

4.1 - RGB Input

The three RGB inputs have to be supplied through coupling capacitors (100 nF).

The maximum input peak-to-peak video amplitude is 1 V.

The input stage includes a clamping function. The clamp uses the input serial capacitor as a ”memory capacitor”.

To avoid a discharge of the serial capacitor during the line (due to leakage current), the input voltage is referenced to the ground.

The clamp is gated by an internally generated ”Back Porch Clamping Pulse” (BPCP). Register 8 allows to choose the way to generate this BPCP (see Figure 1).

When bit 0 is set to 0, the BPCP is synchronized on the trailing or leading edge of HSYNC (Pin 19) (bit 1 = 0: trailing edge, bit 1 = 1: leading edge).

Additionally, the IC automatically works with either positive or negative HSYNC pulses.

– When bit 0 is set to 1, BPCP is synchronized on the leading edge of the blanking pulse BLK (Pin 20). One can use a positive or negative blanking pulse by programming bit 0 in Register 9 (See I^2C Table 3).
– BPCP width can be adjusted with bit 2 and 3 (see Register 8, I^2C table 2).
– If the application already provides the Back Porch Clamping Pulse, bit 4 must be set to 1 (providing a direct connection between Pin 19 and internal BPCP).

4.2 - Synchro Clipping Function

This function is available on channel 2 (Green Channel). When using the Sync On Green (SOG) (Synchro pulse included in the green channel input) the synchro clipping function must be activated (bit 7 set to 1 in register 9) in order to keep the right green output levels and avoid unbalanced colours.

4.3 - Blanking Input

The Blanking pin (FBLK) is TTL compatible.

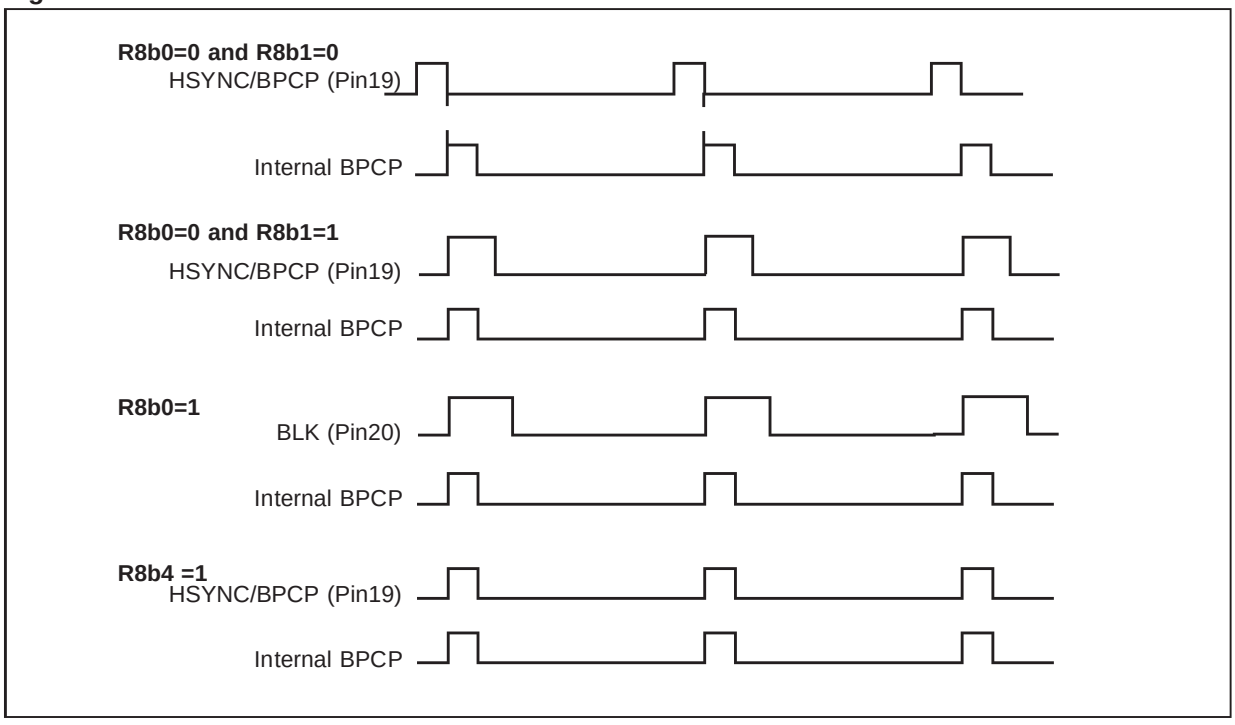
The Blanking pulse can be:

– positive or negative
– line or Composite-type (but not Frame-type).

4.4 - Contrast Adjustment (8 bits)

The contrast adjustment is made by controlling simultaneously the gain of the three internal amplifiers through the I^2C bus interface. Register 1 allows the adjustment in a range of 48 dB.

Figure 1.



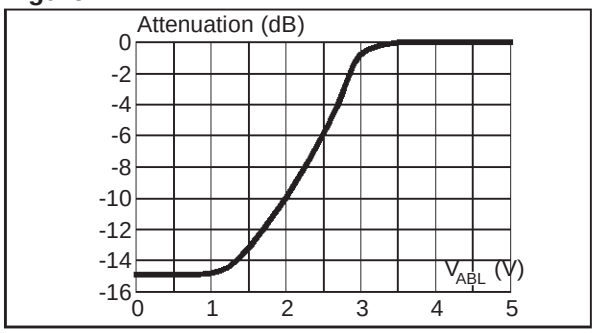
4.5 - ABL Control

The TDA9210 includes an ABL (automatic beam limitation) input to attenuate the RGB Video signals depending on the beam intensity.

The operating range is 2 V (from 3 V to 1 V). A typical 15 dB maximum attenuation is applied to the output signal whatever the contrast adjustment is. (See Figure 2).

When the ABL feature is not used, the ABL input (Pin 2) must be connected to a 5 V supply voltage.

Figure 2.



4.6 - Brightness Adjustment (8 bits)

Brightness adjustment is controlled by the I^2C Bus via Register 2. It consists of adding the same DC voltage to the three RGB signals, after contrast adjustment. When the blanking pulse equals 0, the DC voltage is set to a value which can be adjusted between 0 and 2V with 8mV steps (see Figure 3).

The DC output level is forced to the "Infra Black" level (V_{DC}) when the blanking pulse is equal to 1.

4.7 - Drive Adjustment (3 x 8 bits)

In order to adjust the white balance, the TDA9210 offers the possibility of adjusting separately the overall gain of each channel thanks to the I^2C bus (Registers 3, 4 and 5).

The very large drive adjustment range (48 dB) allows different standards or custom color temperatures.

It can also be used to adjust the output voltages at the optimum amplitude to drive the CRT drivers, keeping the whole contrast control for the end-user only.

The drive adjustment is located after the Contrast, Brightness and OSD switch blocks, so it does not affect the white balance setting when the BRT is adjusted. It also operates on the OSD portion of the signal.

4.8 - OSD Inputs

The TDA9210 allows to mix the OSD signals into the RGB main picture. The four pins dedicated to this function are the following:

– Three TTL RGB inputs (Pins 8, 9, 10) connected to the three outputs of the corresponding OSD processor.

– One TTL fast blanking input (Pin 11) also connected to the FBLK output of the OSD processor.

When a high level is present on the FBLK, the IC acts as follows:

– The three main picture RGB input signals (IN1, IN2, IN3) are internally switched to the internal input clamp reference voltage.

– The three output signals are set to the voltage corresponding to the three OSD input logic states (0 or 1). (See Figure 3).

If the OSD input is at low level, the output and brightness voltages (V_{BRT}) are equal.

If the OSD input is at high level, the output voltage is V_{OSD}, where $V_{OSD} = V_{BRT}$ + OSD and OSD is an I^2C bus-controlled voltage.

OSD varies between 0 V to 4.9 V by 320 mV steps via Register 7 (4 bits). The same variation is applied simultaneously to the three channels providing the OSD contrast.

The grey color can be obtained on output signals when:

– OSD1 = 1, OSD2 = 0 and OSD3 = 1,

– A special bit (bit 5 or 6) in Register 9 is set to 1.

If R9b5 is set to 1, light grey is obtained on output.

If R9b6 is set to 1, dark grey is obtained on output.

In the case where R9b5 and R9b6 are set to 0, the normal operation is provided on output signals.

4.9 - Output Stage

The overall waveforms of the output signal are shown in Figure 3 and Figure 4. The three output stages, which are large bandwidth output amplifiers, are able to deliver up to 4.4 V_{PP} for 0.7 V_{PP} on input.

When a high level is applied on the BLK input (Pin 20), the three outputs are forced to "Infra Black" level (V_{DC}) thanks to a sample and hold circuit (described below).

The black level (which is the output voltage outside the blanking pulse with minimum brightness and no Video input signals) is 400 mV higher than V_{DC}.

The brightness level (V_{BRT}) is then obtained by programming register 2 (see I^2C table 1).

The sample and hold circuit is used to control the "Infra Black" level in the range of 0.5 V to 2.5 V via Register 6 (in case of AC coupling) or Registers 10, 11, 12 (in case of DC coupling) .

This sampling occurs during an internal pulse (OCL) generated inside the blanking pulse window.

Refer to "CRT cathode coupling" part for further details.

Functioning with 5 V Power V_{CC}

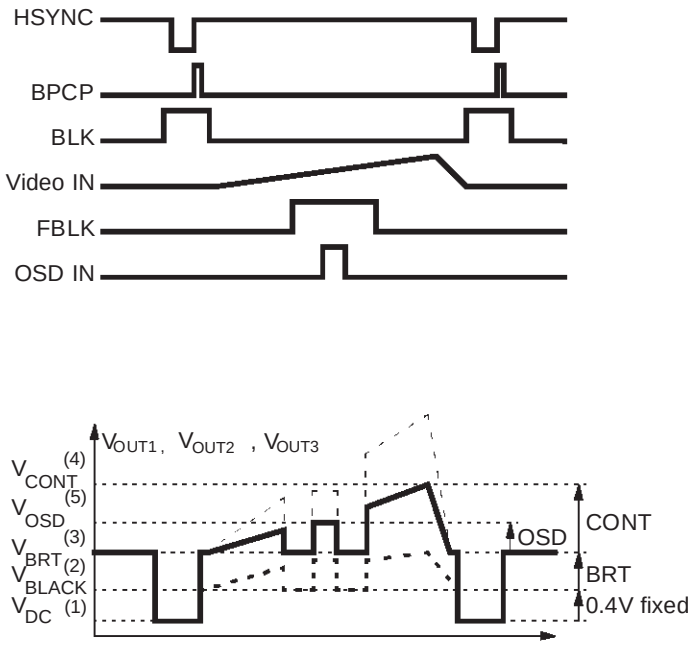
To simplify the application, it is possible to supply the power V_{CC} with 5 V (instead of 8 V nominal) at the expense of output swing voltage.

Functioning without Blanking Pulse

If no blanking pulse is applied to the TDA9210, the internal BPCP can be connected to the sample and hold circuit (Register 8, bit 7 = 1 and BLK pin grounded) so that the output DC level is still controlled by I^2C.

To ensure the device correct behavior in the worst possible conditions, the Brightness Register must be set to 0.

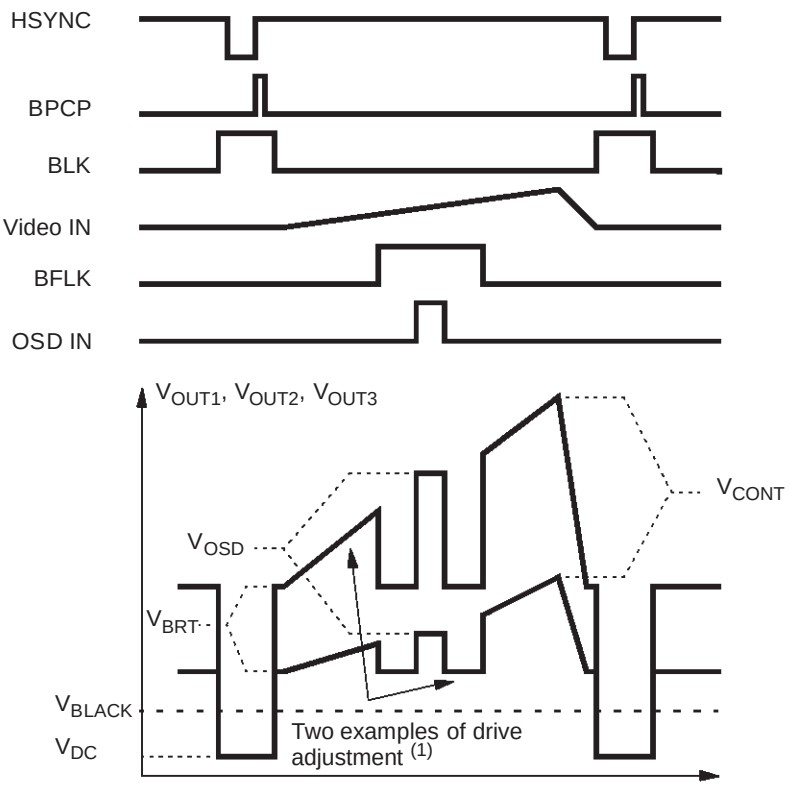
Figure 3. Waveforms VOUT, BRT, CONT, OSD



Notes :

1. V_{DC} = 0.5 to 2.5V
2. V_{BLACK} = V_{DC} + 0.4V
3. V_{BRT} = V_{BLACK} + BRT (with BRT = 0 to 2V)
4. V_{CONT} = V_{BRT} + CONT = k x Video IN (CONT = $4.4V_{PP}$ max. for $V_{IN} = 0.7V_{PP}$)
5. V_{OSD} = V_{BRT} + OSD (OSD max. = $4.9V_{PP}$, OSD min = $0V_{PP}$)

Figure 4. Waveforms (Drive adjustment)



Note :
1.Drive adjustment modifies the following voltages : V_{CONT}, V_{BRT} and V_{OSD}.
Drive adjustment doesn't modify the following voltages : V_{DC} and V_{BLACK}.

4.10 - Bandwidth Adjustment

A new feature: Bandwidth adjustment, has been implemented on the TDA9210.

This function has several advantages:

– Depending on the external capacitive load and on the peak-to-peak output voltage, the bandwidth can be adjusted to avoid any slew-rate phenomenon.

– The preamp bandwidth can be adjusted in order to reduce electromagnetic radiation, since it is possible to slow down the signal rise/fall time at the CRT driver input without too much affecting the rise/fall time at the CRT driver output.

– It is possible to optimize the ratio of the frequency response versus the CRT driver power consumption for any kind of chassis, as the preamp bandwidth adjustment also allows the adjustment of the rise/fall time on the cathode (through the CRT driver).

– In still picture mode, when a high Video swing voltage is of greater interest than rise/fall time, bandwidth adjustment is used to avoid any slew-rate phenomenon at the CRT driver output and to meet electromagnetic radiation requirements.

4.11 - CRT Cathode Coupling (Figure 5)

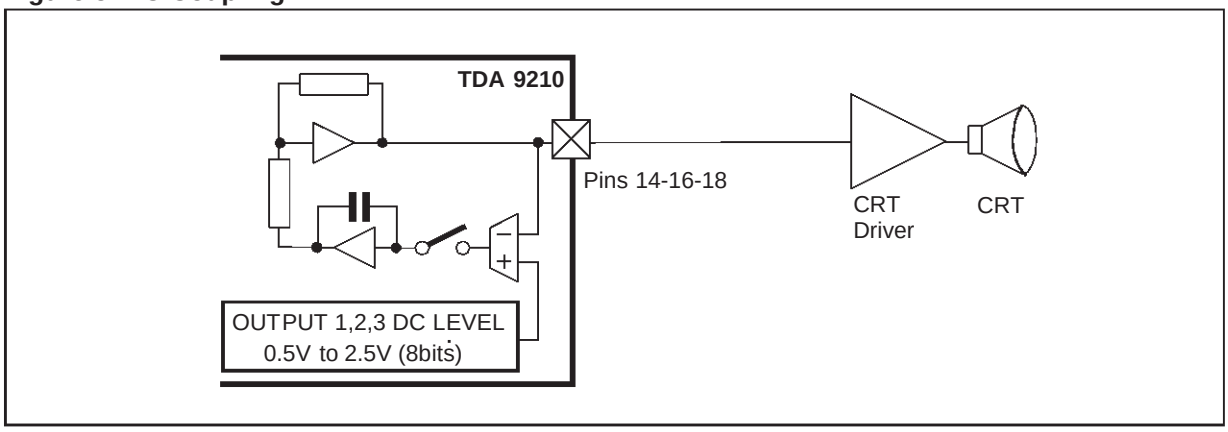
The TDA9210 is designed to be used in DC coupling mode, enabling to build a powerful video system on a small PCB Board and giving a substantial cost saving compared with any other solution available on the market.

The preamplifier outputs control directly the cut-off levels.

The output DC level (VDC) is adjusted independently for each channel from 0.5 V to 2.5 V via registers 10, 11 and 12.

In DC coupling mode, bit 2 must be set to 1 and bit3 to 0 in Register 9.

Figure 5. DC Coupling



4.12 - Stand-by Mode

The TDA9210 has a stand-by mode. As soon as the V_{CC} power (Pin 17) gets lower than 3V (typ.), the device is set in stand-by mode whatever the voltage on analog V_{CCA} (Pin 7) is. The analog blocks are internally switched-off while the logic parts (I^2C bus, power-on reset) are still supplied.

In stand-by mode, the power consumption is below 20 mW.

4.13 - Serial Interface

The 2-wire serial interface is an I^2C interface. The slave address of TDA9210 is DC hex.

A6	A5	A4	A3	A2	A1	A0	W
1	1	0	1	1	1	0	0

The host MCU can write into the TDA9210 registers. Read mode is not available.

In order to write data into the TDA9210, after the "start" message, the MCU must send the following data (see Figure 6):

– the I^2C address slave byte with a low level for the R/W bit,

– the byte to the internal register address where the MCU wants to write data,

– the data.

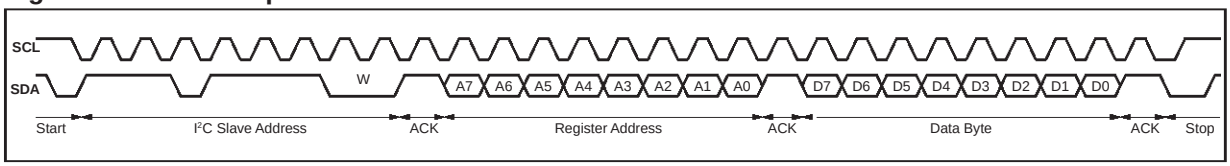
All bytes are sent with MSB bit first. The transfer of written data is ended with a "stop" message.

When transmitting several data, the register addresses and data can be written with no need to repeat the start and slave addresses.

4.14 - Power-on Reset

A power-on reset function is implemented on the TDA9210 so that the I^2C registers have a determined status after power-on. The Power-on reset threshold for a rising supply on V_{CCA} (Pin 7) is 3.8 V (typ.) and 3.2V when the V_{CC} decreases.

Figure 6. I^2C Write Operation



5 - ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Pin	Value	Units
V_{CCA} Max. V_{CCP} Max.	Supply Voltage on Analog V_{CC} Supply Voltage on Power V_{CC}	7 20	5.5 8.8	V V
V_{in} Max.	Voltage at any Input Pins (except Video inputs) and Input/Output Pins	-	5.5	V
V_I Max.	Voltage at Video Inputs	1, 3, 5	1.4	V
T_{stg}	Storage Temperature	-	-	°C
T_{oper}	Operating Junction Temperature	-	+150	°C

6 - THERMAL DATA

Symbol	Parameter	Value	Units
$R_{th(j-a)}$	Max. Junction-ambient Thermal Resistance	69	°C/W
T_j	Typ. Junction Temperature at T_{amb} = 25°C	80	°C

7 - DC ELECTRICAL CHARACTERISTICS

T_{amb} = 25°C, V_{CCA} = 5V, V_{CCP} = 8V, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{CCA}	Analog Supply Voltage	Pin 7	4.5	5	5.5	V
V_{CCP}	Power Supply Voltage	Pin 17	4.5	8	8.8	V
I_{CCA}	Analog Supply Current	V_{CCA} = 5V		70		mA
I_{CCP}	Power Supply Current	V_{CCP} = 8V		55		mA
V_I	Video Input Voltage Amplitude			0.7	1	V
Vo	Output Voltage Range		0.5		V_{CCP} -0.5V	V
V_{IL} V_{IH}	Low Level Input Voltage High Level Input Voltage	OSD, FBLK, BLK, HSYNC	 2.4		0.8	V V
I_{IN}	Input Current	OSD, FBLK, BLK	-1		1	µA
R_{HS}	Input Resistor	HSYNC		40		kΩ

8 - AC ELECTRICAL CHARACTERISTICS

T_{amb} = 25°C, V_{CCA} = 5V, V_{CCP}= 8V, V_i = 0.7 V_{PP}, C_{LOAD} = 5pF
R_S = 100Ω, serial between output pin and C_{LOAD}, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
VIDEO INPUTS (PINS 1, 3, 5)						
V_I	Video Input Voltage Amplitude	Max. Contrast and Drive		0.7	1	V
VIDEO OUTPUT SIGNAL (PINS 14, 16, 18) - GENERAL						
GAM	Maximum Gain	Max Contrast and Drive (CRT = DRV = 254 dec)		16		dB
VOM	Maximum Video Output Voltage (Note 1)	Max Contrast and Drive (CRT = DRV = 254 dec)		4.4		V
VON	Nominal Video Output Voltage	Contrast and Drive at POR (CRT = DRV = 180 dec)		2.2		V
CAR	Contrast Attenuation Range	From max. Contrast (CRT=254 dec) to min. Contrast (CRT = 1 dec)		48		dB
DAR	Drive Attenuation Range	From Max. Drive (DRV = 254 dec) to min Drive (DRV = 1 dec)		48		dB
GM	Gain Matching	Contrast and Drive at POR		±0.1		dB
t_R, t_F	Rise Time, Fall Time (Note 2)	V_{OUT} = 2 V_{PP} (BW = 15 dec) V_{OUT} = 2 V_{PP} (BW = 0 dec)		2.7 4.3		ns ns
BW	Large Signal Bandwidth	V_{OUT} = 2 V_{PP}		130		MHz
BW	Bandwidth Adjustment Range	V_{OUT} = 2 V_{PP} Minimum bandwidth (BW = 0 dec) Maximum bandwidth (BW =15 dec)		 80 130		 MHz MHz
CT	Crosstalk between Video Outputs	V_{OUT} = 2 V_{PP} @ f = 10 MHz @ f = 50 MHz		60 35		dB dB
VIDEO OUTPUT SIGNAL — BRIGHTNESS						
BRTmax	Maximum Brightness Level	Max. Brightness (BRT = 255 dec) and Max. Drive (DRV = 254 dec)		2		V
BRTmin	Minimum Brightness Level	Min. Brightness (BRT = 0 dec) and Max. Drive (DRV = 254 dec)		0		V
VIP	Insertion Pulse			0.4		V
BRTM	Brightness Matching	Brightness and Drive at POR		±10		mV
VIDEO OUTPUT SIGNAL — OSD						
 OSDmax OSDmin	 Maximum OSD Output Level Minimum OSD Output Level	Max. Drive (DRV = 254 dec) Max. OSD (OSD = 15 dec) Min. OSD (OSD = 0 dec)		 4.9 0		 V V
VIDEO OUTPUT SIGNAL — DC LEVEL (DC COUPLING MODE)						
DCLmax DCLmin	Maximum Output DC Level Minimum Output DC Level	Max. Cut-off (Cut-off = 255 dec) Min. Cut-off (Cut-off = 40 dec)		2.5 0.4		V V
DCLstep	Output DC Level Step			10		mV
DCLTD	Output DC Level Drift	Tj variation=100°C		0.5		%

Note 1 : Assuming that V_{OM} remains within the range of Vo (between 0.5V and V_{CCP} - 0.5V)
Note 2 : t_R, t_F are calculated values, assuming an ideal input rise/fall time of 0ns ($t_R = \sqrt{t_{ROUT}^2 + t_{RIN}^2}$, $t_F = \sqrt{t_{FOUT}^2 + t_{FIN}^2}$

AC ELECTRICAL CHARACTERISTICS

T_{amb} = 25°C, V_{CCA} = 5V, V_{CCP}= 8V, V_i = 0.7 V_{PP}, C_{LOAD} = 5 pF, unless otherwise specified

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
ABL (PIN 2)						
GABLmin GABLmax	ABL Mini Attenuation ABL Maxi Attenuation	V_{ABL}≥3.2 V V_{ABL} = 1 V		0 15		dB dB
V_{ABL}	ABL Threshold Voltage	For output attenuation		3		V
IABLhigh IABLlow	High ABL Input Current Low ABL Input Current	V_{ABL} = 3.2V V_{ABL} = 1V		0 -2		µA µA

9 - I²C ELECTRICAL CHARACTERISTICS

T_{amb} = 25°C, V_{CCA} = 5V, unless otherwise specified

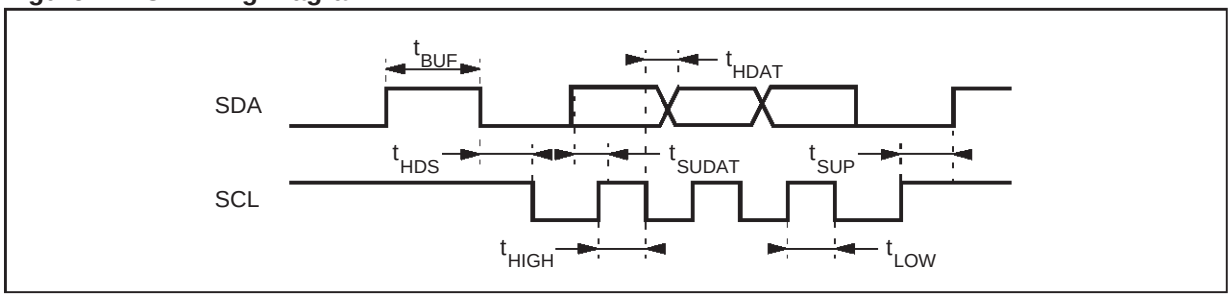
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{IL}	Low Level Input Voltage	On Pins SDA, SCL			1.5	V
V_{IH}	High Level Input Voltage		3			V
I_{IN}	Input Current (Pins SDA, SCL)	0.4 V < V_{IN} < 4.5 V	-10		+10	µA
$f_{SCL(Max.)}$	SCL Maximum Clock Frequency		200		0.25	kHz
V_{OL}	Low Level Output Voltage	SDA Pin when ACK Sink Current = 6mA			0.6	V

10 - I²C INTERFACE TIMING REQUIREMENTS

(see Figure 11)

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{BUF}	Time the bus must be free between two accesses	1300			ns
t_{HDS}	Hold Time for Start Condition	600			ns
t_{SUP}	Set-up Time for Stop Condition	600			ns
t_{LOW}	The Low Period of Clock	1300			ns
t_{HIGH}	The High Period of Clock	600			ns
t_{HDAT}	Hold Time Data	300			ns
t_{SUDAT}	Set-up Time Data	250			ns
t_R, t_F	Rise and Fall Time of both SDA and SCL	20		300	ns

Figure 7. I²C Timing Diagram



11 - I²C REGISTER DESCRIPTION

Register Sub-addressed - I²C Table 1

Sub-address		Register Names		POR Value		Max. Value	
Hex	Dec			Hex	Dec	Hex	Dec
01	01	Contrast (CRT)	8-bit DAC	B4	180	FE	254
02	02	Brightness (BRT)	8-bit DAC	B4	180	FF	255
03	03	Drive 1 (DRV)	8-bit DAC	B4	180	FE	254
04	04	Drive 2 (DRV)	8-bit DAC	B4	180	FE	254
05	05	Drive 3 (DRV)	8-bit DAC	B4	180	FE	254
06	06	Not Used		-	-	-	-
07	07	OSD Contrast (OSD)	4-bit DAC	09	09	0F	15
08	08	BPCP & OCL	Refer to the I²C table 2	04	04		
09	09	Miscellaneous	Refer to the I²C table 3	1C	28		
0A	10	Cut Off Out 1 DC Level (Cut-off)	8-bit DAC	B4	180	FF	255
0B	11	Cut Off Out 2 DC Level (Cut-off)	8-bit DAC	B4	180	FF	255
0C	12	Cut Off Out 3 DC Level (Cut-off)	8-bit DAC	B4	180	FF	255
0D	13	Bandwidth Adjustment (BW)	4-bit DAC	07	07	0F	15

For Contrast & Drive adjustment, code 00 (dec) and 255 (dec) are not allowed.
For Output DC Level, code 00(dec), 01(dec), 02(dec) are not allowed (Register 06).
For Cut Off Output DC Level, output voltage is linear between code 10 and code 235 (Registers 0A, 0B, 0C).

BPCP & OCL Register (R8) - I²C Table 2 (see also Figure 8)

b7	b6	b5	b4	b3	b2	b1	b0	Function	POR Value
			0				0	Internal BPCP triggered by HSYNC	x
			0				1	Internal BPCP triggered by BLK	
			0			0		Internal BPCP synchronized by the trailing edge	x
			0			1		Internal BPCP synchronized by the leading edge	
			0	0	0			Internal BPCP Width = 0.33 µs	
			0	0	1			Internal BPCP Width = 0.66 µs	x
			0	1	0			Internal BPCP Width = 1 µs	
			0	1	1			Internal BPCP Width = 1.33 µs	
			1					Internal BPCP = BPCP input (Pin 23)	
		0						Normal Operation	x
		1						Reserved (Force BPCP to 1 in test)	
	0							Normal Operation	x
	1							Reserved (Force OCL to 1 in test)	
0								Internal OCL pulse triggered by BLK (pin 24)	x
1								Internal OCL pulse = Internal BPCP	

Miscellaneous Register (R9) - I²C Table 3

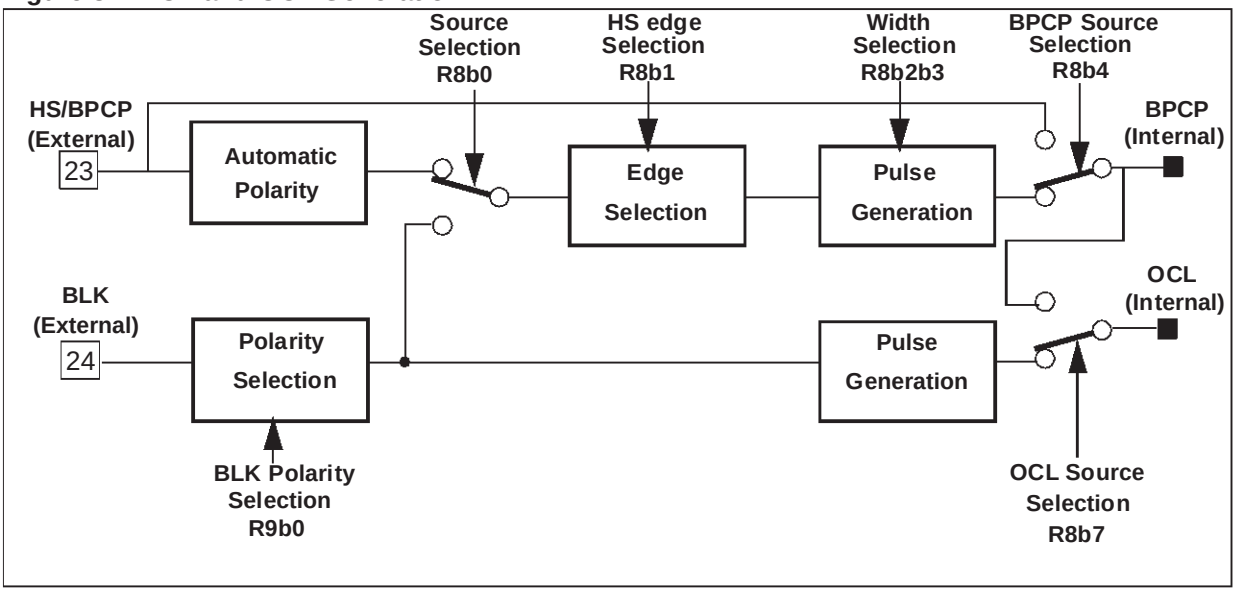
b7	b6	b5	b4	b3	b2	b1	b0	Function	POR Value
							0	Positive Blanking Polarity	x
							1	Negative Blanking Polarity	
						0		Soft Blanking = OFF	x
						1		Soft Blanking = ON	
			x	0	1			DC Coupling Mode (Note 3)	
	0	0						Light Grey on OSD Outputs = OFF	x
	0	1						Light Grey on OSD Outputs = ON	
	0	0						Dark Grey on OSD Outputs = OFF	x
	1	0						Dark Grey on OSD Outputs = ON	
0								SOG Clipping = OFF	x
1								SOG Clipping = ON	

Note 3 : After Power ON, the DC coupling mode must be programmed in Register 9 by setting bit2=1 and bit3=0.

Bandwidth Adjustment (R13) - I²C Table 4

b7	b6	b5	b4	b3	b2	b1	b0	Function	POR Value
				1	1	1	1	130 MHz	
				0	1	1	1	100 MHz	x
				0	0	0	0	80 MHz	
		0	0					Normal Operation	x
		0	1					BW DAC output connected to BLK input (for test)	
		1	0					BW DAC complementary output connected to BLK input (for test)	

Figure 8. BPCP and OCL Generation



12 - INTERNAL SCHEMATICS

Figure 9.

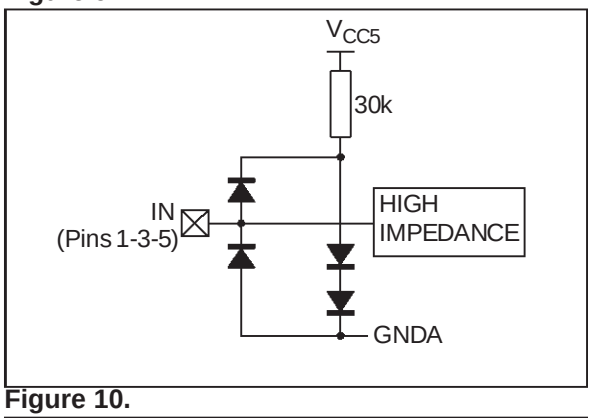


Figure 10.

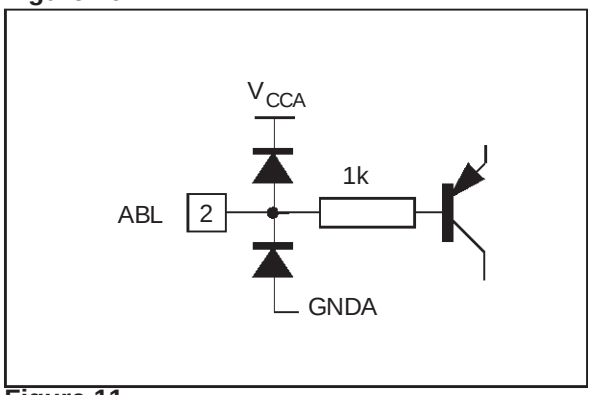


Figure 11.

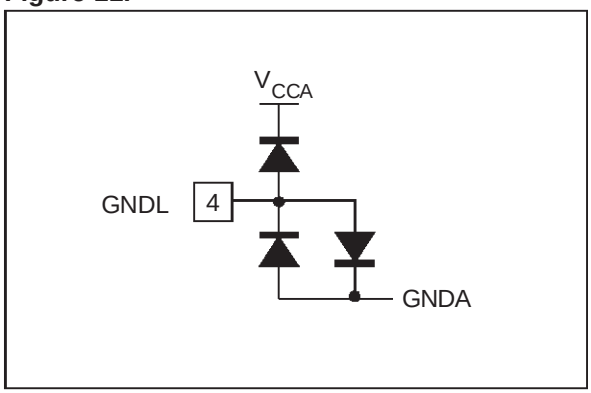


Figure 12.

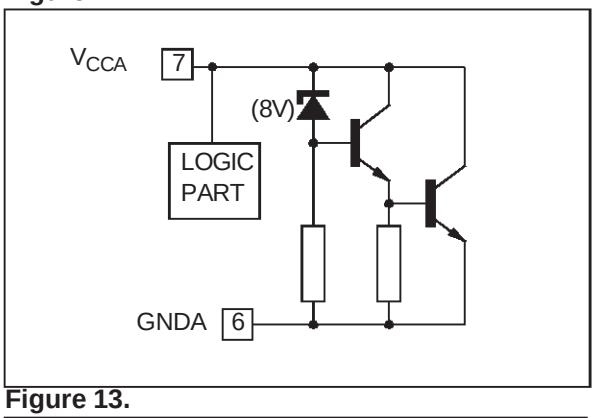


Figure 13.

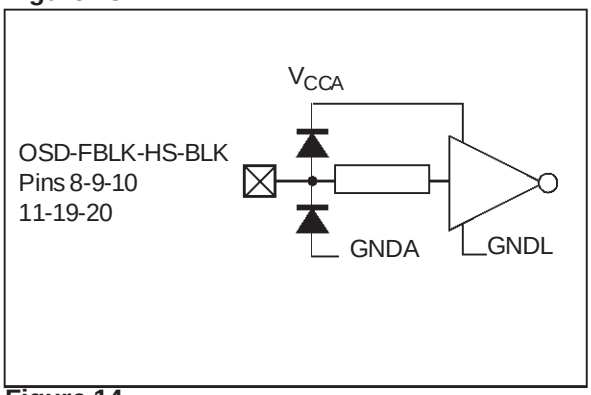


Figure 14.

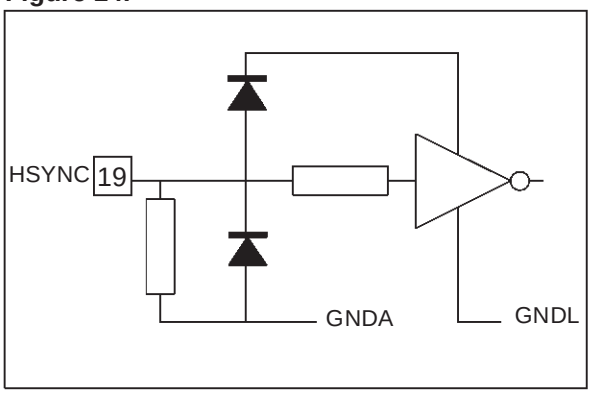


Figure 15.

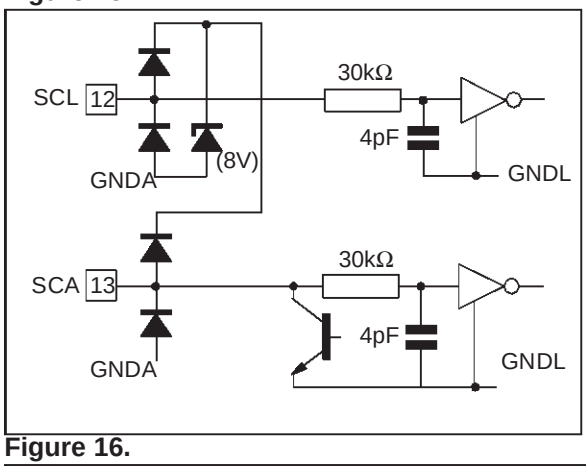


Figure 16.

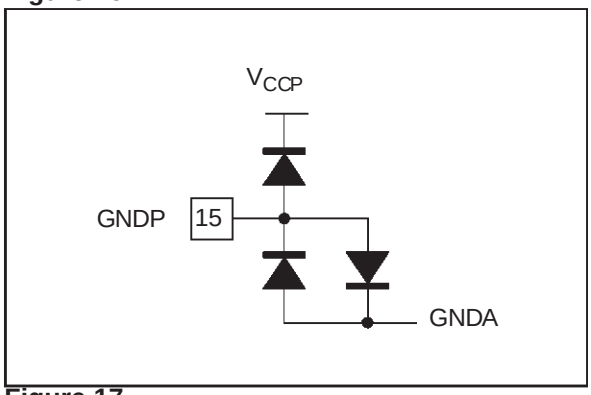


Figure 17.

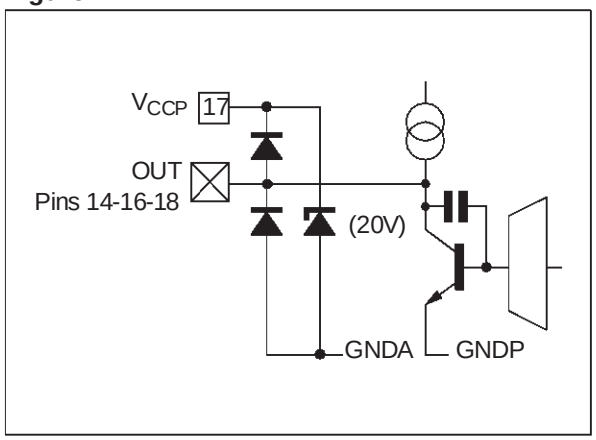


Figure 18. TDA9210 - TDA9535/9536 Demonstration Board: Silk Screen and Trace (scale 1:1)

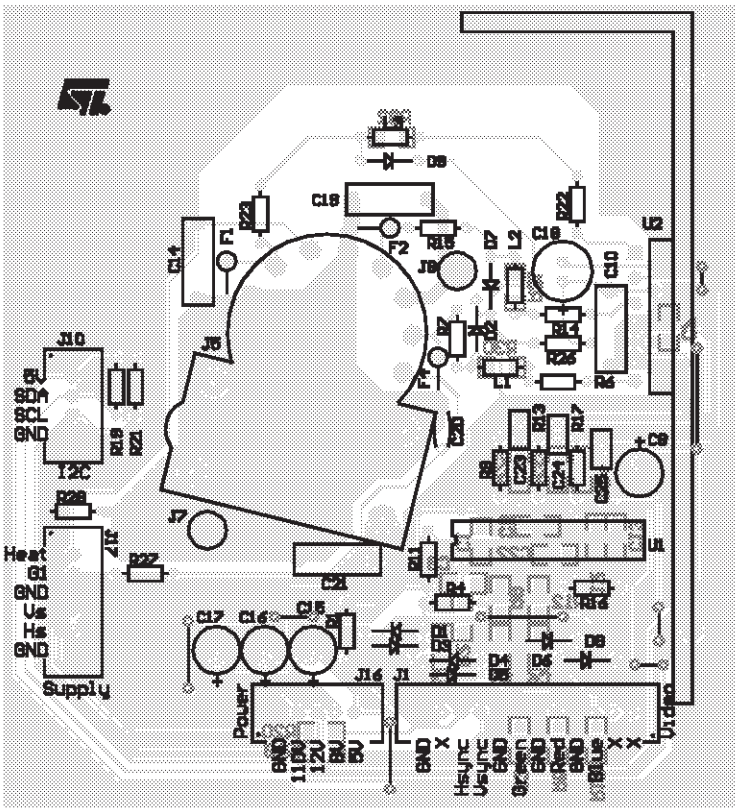
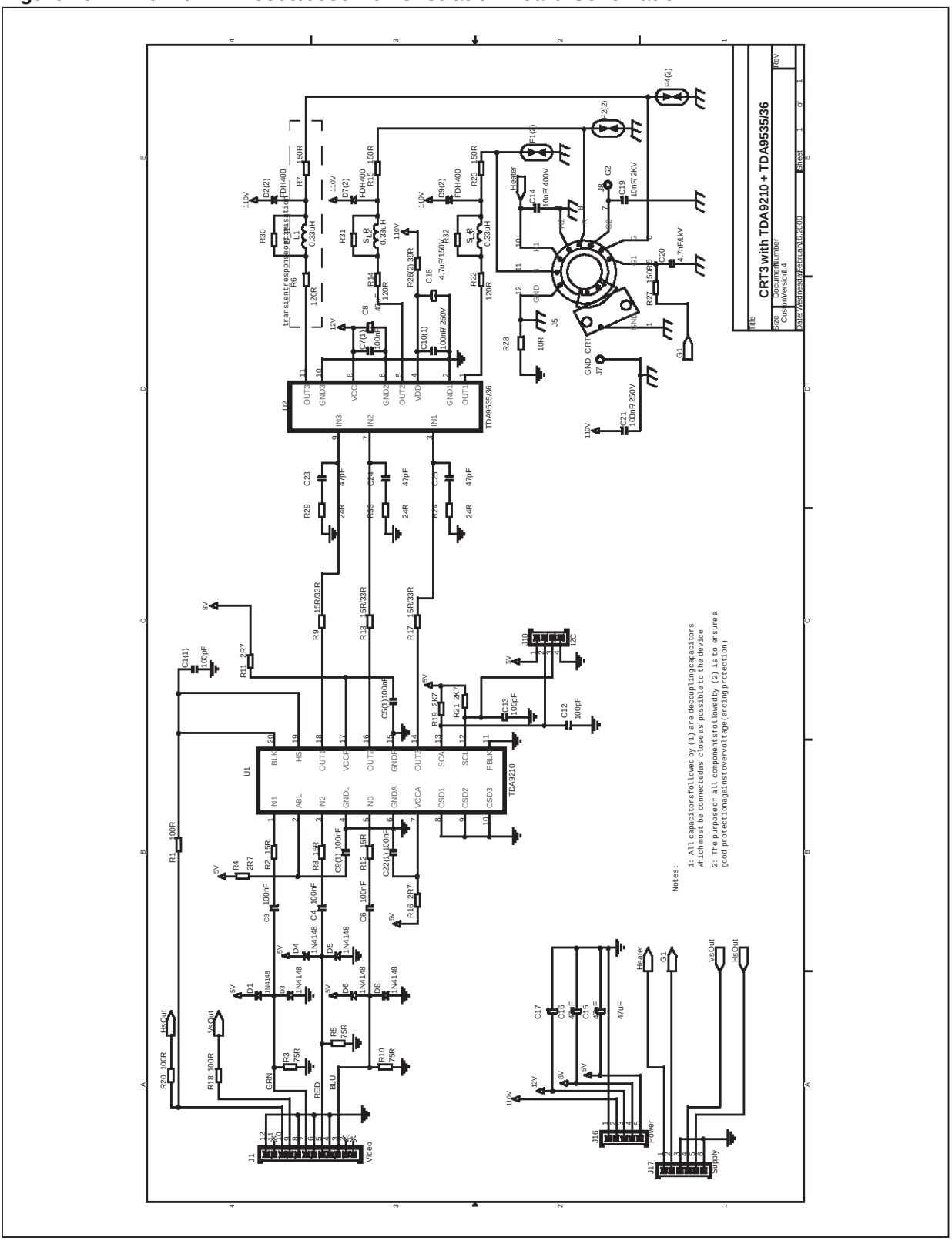
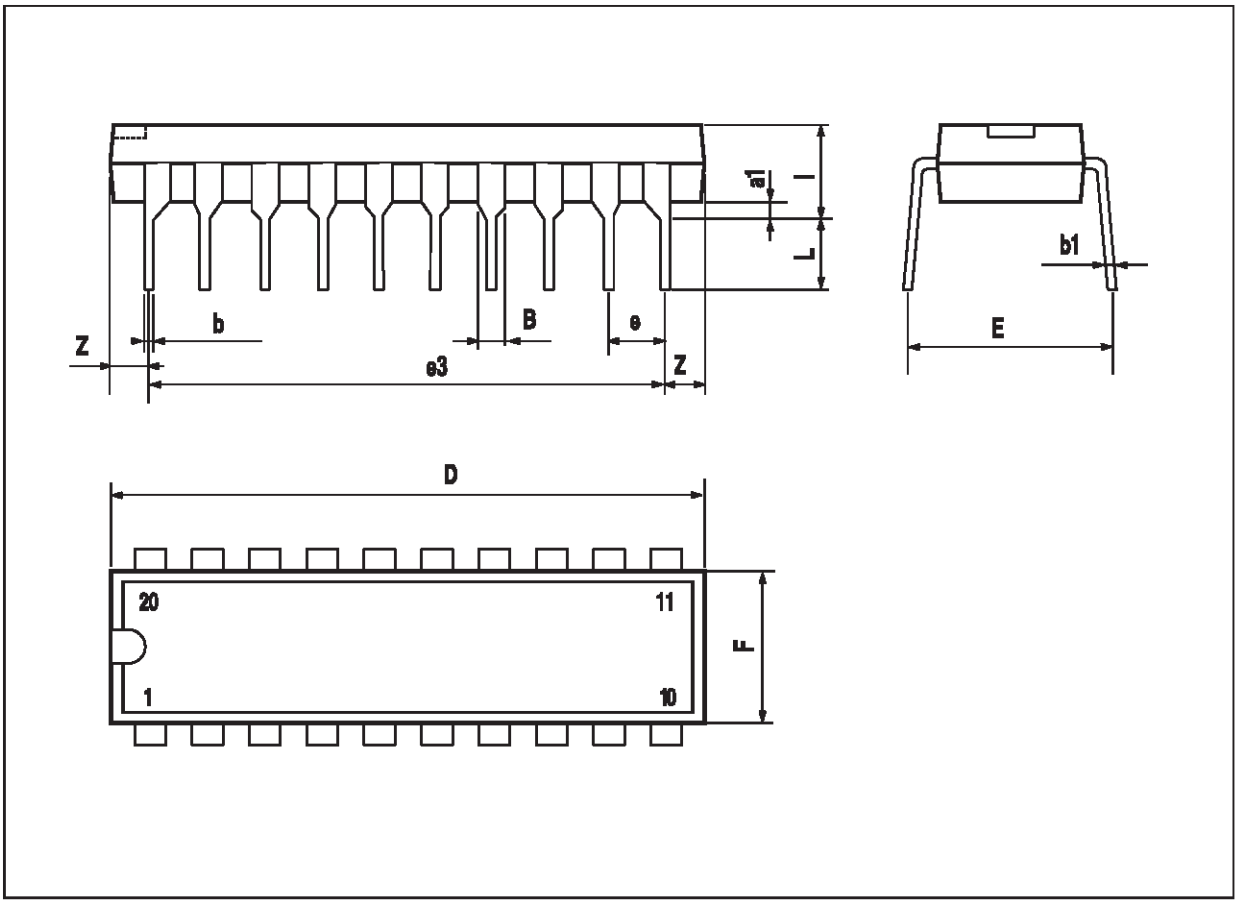


Figure 19. TDA9210 - TDA9535/9536 Demonstration Board Schematic



13 - PACKAGE MECHANICAL DATA

20 Pins — Plastic Dip



Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
a1	0.254			0.010		
B	1.39		1.65	0.055		0.065
b		0.45			0.018	
b1		0.25			0.010	
D			25.4			1.000
E		8.5			0.335	
e		2.54			0.100	
e3		22.86			0.900	
F			7.1			0.280
I			3.93			0.155
L		3.3			0.130	
Z			1.34			0.053