

TOSHIBA MOS MEMORY PRODUCTS

262,144 WORD×1 BIT DYNAMIC RAM
SILICON MONOLITHIC
N-CHANNEL SILICON GATE MOS

TMM41256AP/AT/AZ-10, TMM41256AP/AT/AZ-12
TMM41256AP/AT/AZ-15

DESCRIPTION

The TMM41256AP/AT/AZ is the N-channel dynamic RAM organized 262,144 words by 1 bit. Multiplexed address inputs permit the TMM41256AP/AT/AZ to be packaged in a standard 16 pin plastic DIP, 18 pin PLCC and 16 pin ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. The double layered MOS technology with polycide and poly Si permits the TMM41256AP/AT/AZ high speed operation.

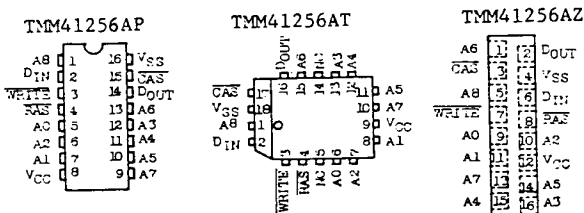
FEATURES

- 262,144 words by 1 bit organization
- Fast access time and cycle time

	TMM41256AP/AT/AZ-10/12/15
RAS Access Time	100ns/120ns/150ns
CAS Access Time	50ns/ 60ns/ 75ns
Cycle Time	190ns/220ns/260ns

- Single power supply of $5V \pm 10\%$ with a built-in V_{BB} generator
- Low Power:
 - 440mW MAX. Operating (TMM41256AP/AT/AZ-10)
 - 396mW MAX. Operating (TMM41256AP/AT/AZ-12)
 - 358mW MAX. Operating (TMM41256AP/AT/AZ-15)
 - 28mW MAX. Standby

PIN CONNECTION (TOP VIEW)



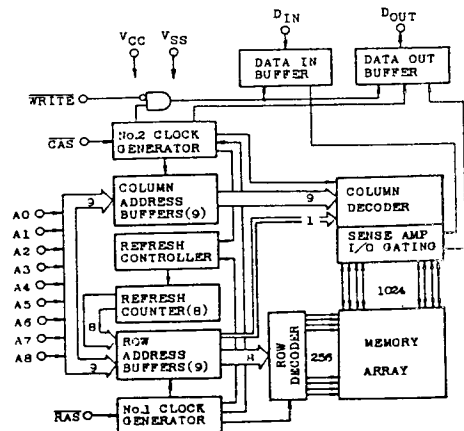
PIN NAMES

A0 ~ A8	Address Inputs
CAS	Column Address Strobe
D1N	Data In
DOUT	Data Out
RAS	Row Address Strobe
WRITE	Read/Write Input
VCC	Power (+5V)
VSS	Ground

Also, the advanced circuit techniques have realized low power dissipation. System oriented features include single power supply of $5V \pm 10\%$ tolerance, direct interfacing capability with high performance logic families such as schottky TTL. In addition to the \overline{RAS} only refresh mode and a \overline{CAS} before \overline{RAS} automatic refresh are available. Another special feature of TMM41256AP/AT/AZ is page mode, allowing the user to access at a high data rate.

- Output unlatched at cycle end allows two-dimensional chip selection
- Common I/O capability using "EARLY WRITE" operation
- Read-Modify-Write, \overline{CAS} before \overline{RAS} refresh, \overline{RAS} -only refresh, Hidden refresh, and Page Mode capability
- All inputs and output TTL compatible
- 256 refresh cycles/4ms
- Package
 - Plastic DIP : TMM41256AP
 - Plastic Leaded Chip Carrier: TMM41256AT
 - Plastic ZIP : TMM41256AZ

BLOCK DIAGRAM



TMM41256AP/AT/AZ-10, TMM41256AP/AT/AZ-12 TMM41256AP/AT/AZ-15

ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input and Output Voltage	V_{IN}, V_{OUT}	-1 ~ 7	V	1
Power Supply Voltage	V_{CC}	-1 ~ 7	V	
Operating Temperature	T_{OPR}	0 ~ 70	°C	
Storage Temperature	T_{STG}	-55 ~ 150	°C	
Soldering Temperature • Time	T_{SOLDER}	260 • 10	°C • sec	
Power Dissipation	P_D	600	mW	
Short Circuit Output Current	I_{OUT}	50	mA	

RECOMMENDED DC OPERATING CONDITIONS ($T_a = 0 \sim 70^\circ\text{C}$)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	—	6.5	V	
V_{IL}	Input Low Voltage	-1.0	—	0.8	V	

DC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V \pm 10\%$, $T_a = 0 \sim 70^\circ\text{C}$)

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	NOTES	
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current (RAS, CAS Cycling: $t_{RC} = t_{RCMIN.}$)	TMM41256AP/AT/AZ-10	—	80	mA	3, 4
		TMM41256AP/AT/AZ-12	—	72	mA	
		TMM41256AP/AT/AZ-15	—	65	mA	
I_{CC2}	STANDBY CURRENT Power Supply Standby Current (RAS = CAS = V_{IH})	—	5	mA		
I_{CC3}	RAS ONLY REFRESH CURRENT Average Power Supply Current, RAS Only Refresh Mode (RAS Cycling, CAS = V_{IH} : $t_{RC} = t_{RCMIN.}$)	TMM41256AP/AT/AZ-10	—	70	mA	3
		TMM41256AP/AT/AZ-12	—	62	mA	
		TMM41256AP/AT/AZ-15	—	55	mA	
I_{CC4}	PAGE MODE CURRENT Average Power Supply Current, Page Mode (RAS = V_{IL} , CAS Cycling: $t_{PC} = t_{PCMIN.}$)	TMM41256AP/AT/AZ-10	—	60	mA	3, 4
		TMM41256AP/AT/AZ-12	—	55	mA	
		TMM41256AP/AT/AZ-15	—	50	mA	
I_{CC5}	CAS BEFORE RAS REFRESH CURRENT Average Power Supply Current, CAS Before RAS Refresh Mode (RAS, CAS Cycling, CAS Before RAS: $t_{RC} = t_{RCMIN.}$)	TMM41256AP/AT/AZ-10	—	70	mA	3
		TMM41256AP/AT/AZ-12	—	62	mA	
		TMM41256AP/AT/AZ-15	—	55	mA	
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input ($0V \leq V_{IN} \leq 6.5V$, ALL Other Pins Not Under Test = 0V)	-10	10	μA		
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, $0V \leq V_{OUT} \leq +5.5V$)	-10	10	μA		
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage ($I_{OUT} = -5\text{mA}$)	2.4	—	V		
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage ($I_{OUT} = 4.2\text{mA}$)	—	0.4	V		

TMM41256AP/AT/AZ-10, TMM41256AP/AT/AZ-12 TMM41256AP/AT/AZ-15

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

SYMBOL	PARAMETER	TMM41256AP/ AT/AZ-10		TMM41256AP/ AT/AZ-12		TMM41256AP/ AT/AZ-15		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t _{RC}	Random Read or Write Cycle Time	190	—	220	—	260	—	ns	
t _{RWC}	Read-Write Cycle Time	200	—	240	—	285	—	ns	
t _{RMW}	Read-Modify-Write Cycle Time	220	—	260	—	310	—	ns	
t _{PC}	Page Mode Cycle Time	100	—	120	—	145	—	ns	
t _{PRWC}	Page Mode Read-Write Cycle Time	110	—	140	—	170	—	ns	
t _{PRMW}	Page Mode Read-Modify Write Cycle Time	130	—	160	—	195	—	ns	
t _{RAC}	Access Time from $\overline{\text{RAS}}$	—	100	—	120	—	150	ns	8, 10
t _{CAC}	Access Time from $\overline{\text{CAS}}$	—	50	—	60	—	75	ns	9, 10
t _{OFF}	Output Buffer Turn-Off Delay	5	25	5	30	5	35	ns	11
t _T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	7
t _{RP}	$\overline{\text{RAS}}$ Precharge Time	80	—	90	—	100	—	ns	
t _{RAS}	$\overline{\text{RAS}}$ Pulse Width	100	10,000	120	10,000	150	10,000	ns	
t _{RSH}	$\overline{\text{RAS}}$ Hold Time	50	—	60	—	75	—	ns	
t _{CSH}	$\overline{\text{CAS}}$ Hold Time	100	—	120	—	150	—	ns	
t _{CAS}	$\overline{\text{CAS}}$ Pulse Width	50	10,000	60	10,000	75	10,000	ns	
t _{RCD}	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	25	50	25	60	25	75	ns	13
t _{CRP}	$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	10	—	10	—	10	—	ns	
t _{CPN}	$\overline{\text{CAS}}$ Precharge Time	15	—	20	—	25	—	ns	
t _{CP}	Page Mode $\overline{\text{CAS}}$ Precharge Time	40	—	50	—	60	—	ns	
t _{ASR}	Row Address Set-Up Time	0	—	0	—	0	—	ns	
t _{RAH}	Row Address Hold Time	15	—	15	—	15	—	ns	
t _{ASC}	Column Address Set-Up Time	0	—	0	—	0	—	ns	
t _{CAH}	Column Address Hold Time	20	—	25	—	30	—	ns	
t _{AR}	Column Address Hold Time Reference to $\overline{\text{RAS}}$	70	—	85	—	105	—	ns	
t _{RCS}	Read Command Set-Up Time	0	—	0	—	0	—	ns	
t _{RCH}	Read Command Hold Time Reference to $\overline{\text{CAS}}$	0	—	0	—	0	—	ns	12
t _{RRH}	Read Command Hold Time Reference to $\overline{\text{RAS}}$	10	—	15	—	20	—	ns	12
t _{WCH}	Write Command Hold Time	20	—	25	—	30	—	ns	
t _{WCR}	Write Command Hold Time Reference to $\overline{\text{RAS}}$	70	—	85	—	105	—	ns	
t _{WP}	Write Command Pulse Width	20	—	25	—	30	—	ns	
t _{RWL}	Write Command to $\overline{\text{RAS}}$ Lead Time	25	—	35	—	45	—	ns	
t _{CWL}	Write Command to $\overline{\text{CAS}}$ Lead Time	25	—	35	—	45	—	ns	
t _{DS}	Data-In Set-Up Time	0	—	0	—	0	—	ns	14
t _{DH}	Data-In Hold Time	20	—	25	—	30	—	ns	14
t _{DHR}	Data-In Hold Time Reference to $\overline{\text{RAS}}$	70	—	85	—	105	—	ns	
t _{REF}	Refresh Period	—	4	—	4	—	4	ms	
t _{WCS}	Write Command Set-Up Time	0	—	0	—	0	—	ns	15

TMM41256AP/AT/AZ-10, TMM41256AP/AT/AZ-12 TMM41256AP/AT/AZ-15

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

SYMBOL	PARAMETER	TMM41256AP/ AT/AZ-10		TMM41256AP/ AT/AZ-12		TMM41256AP/ AT/AZ-15		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t _{CWD}	CAS to WRITE Delay Time	30	—	40	—	50	—	ns	15
t _{RWD}	RAS to WRITE Delay Time	80	—	100	—	125	—	ns	15
t _{CSR}	CAS Set-Up Time (CAS before RAS)	10	—	10	—	10	—	ns	
t _{CHR}	CAS Hold Time (CAS before RAS)	30	—	30	—	30	—	ns	
t _{RPC}	RAS Precharge to CAS Active Time	0	—	0	—	0	—	ns	
t _{CPT}	CAS Precharge Time (CAS before RAS Counter Test)	40	—	50	—	60	—	ns	

CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, T_a = 0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
C _{I1}	Input Capacitance (A ₀ ~ A ₈ , D _{IN})	—	5	pF
C _{I2}	Input Capacitance (RAS, CAS, WRITE)	—	7	
C _O	Output Capacitance (D _{OUT})	—	7	

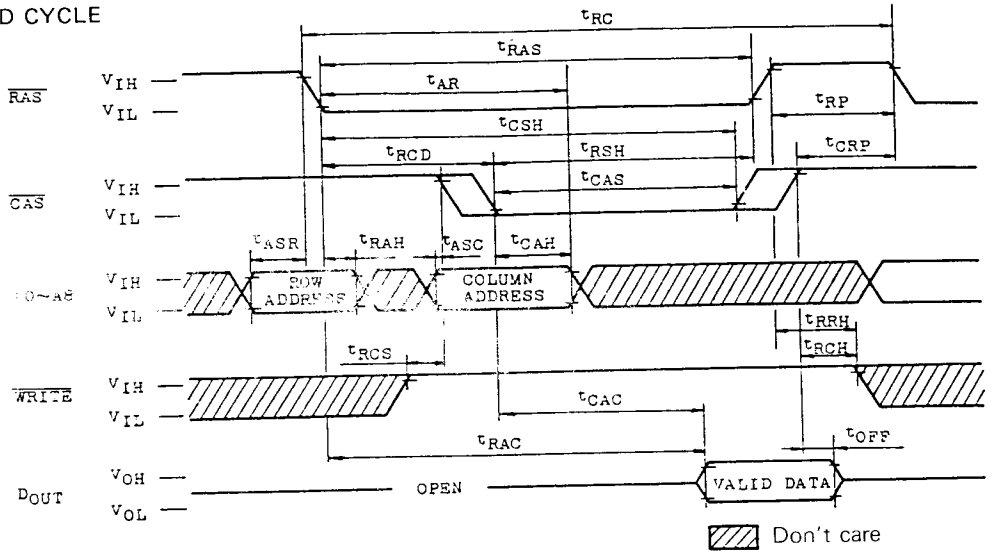
NOTES:

- Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
- All voltages are referenced to V_{SS}.
- I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} depend on cycle rate.
- I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
- An initial pause of 200μs is required after power-up followed by any 8 RAS cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 CAS Before RAS initialization cycles instead of 8 RAS cycles are required.
- AC measurements assume t_T = 5ns.
- V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
- Assumes that t_{RCD} ≤ t_{RCD} (max.). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
- Assume that t_{RCD} ≥ t_{RCD} (max.).
- Measured with a load equivalent to 2 TTL loads and 100pF.
- t_{OFF} (max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
- Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
- Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
- These parameters are referenced to $\overline{\text{CAS}}$ leading edge in early write cycles and to $\overline{\text{WRITE}}$ leading edge in read-write or read-modify-write cycles.
- t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If t_{WCS} ≥ t_{WCS} (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; If t_{CWD} ≥ t_{CWD} (min.) and t_{RWD} ≥ t_{RWD} (min.), the cycle is a read-write cycle or read-modify-write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

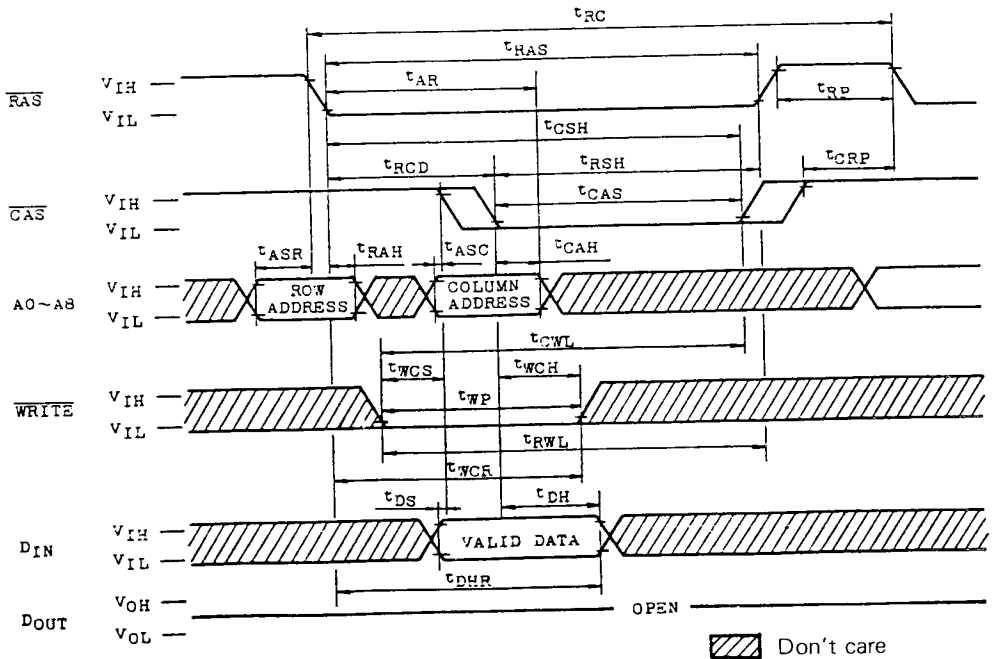
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TIMING WAVEFORMS

● READ CYCLE

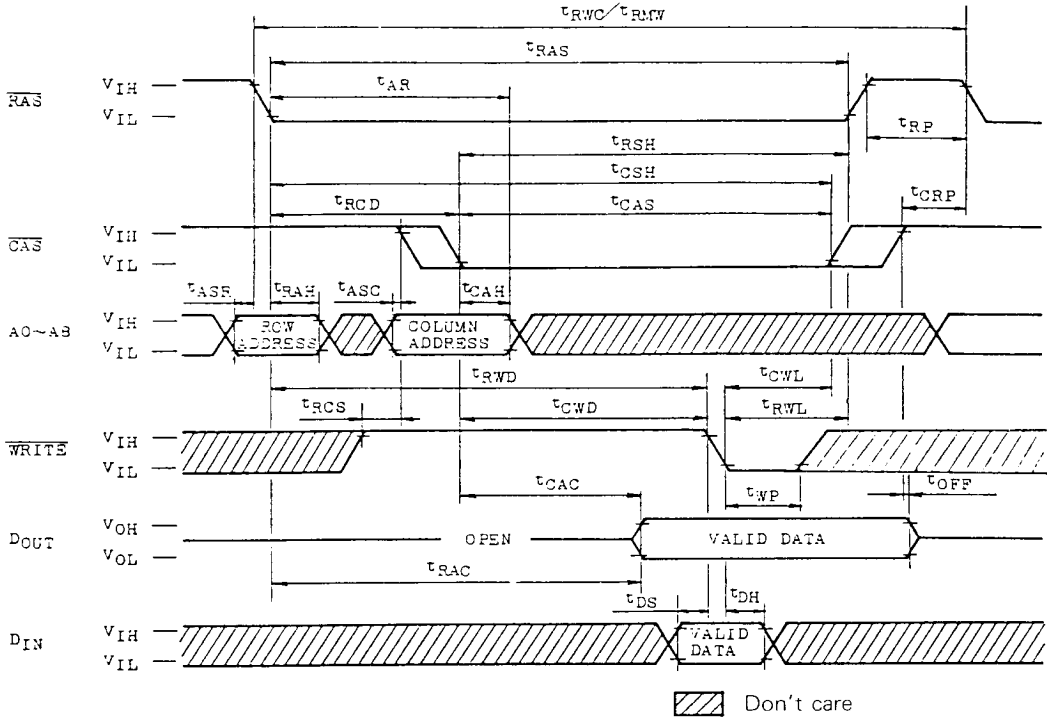


● WRITE CYCLE (EARLY WRITE)



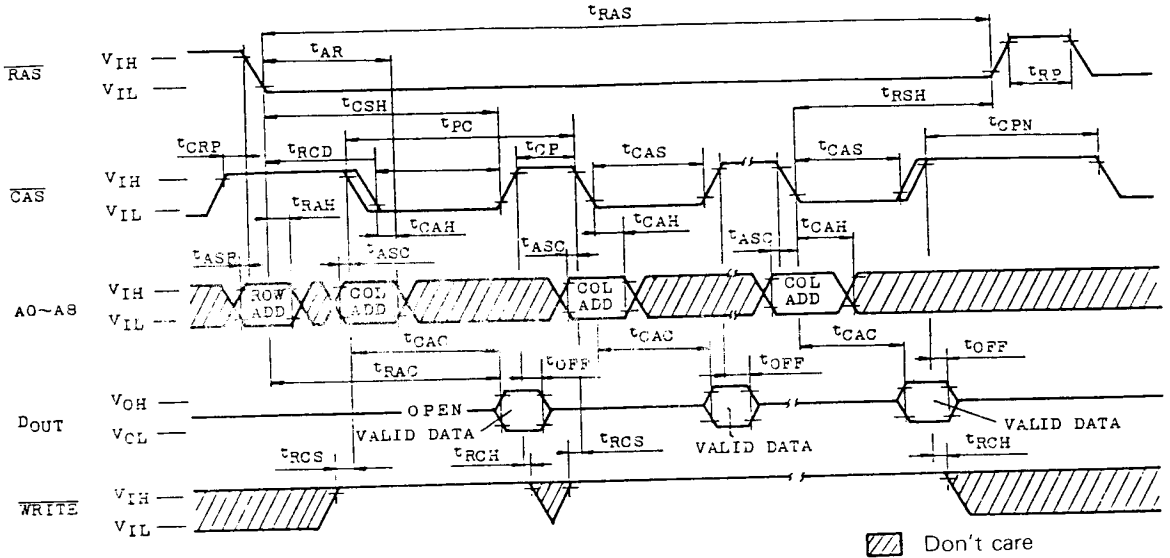
TMM41256AP/AT/AZ-10, TMM41256AP/AT/AZ-12 TMM41256AP/AT/AZ-15

- READ-WRITE/READ-MODIFY-WRITE CYCLE

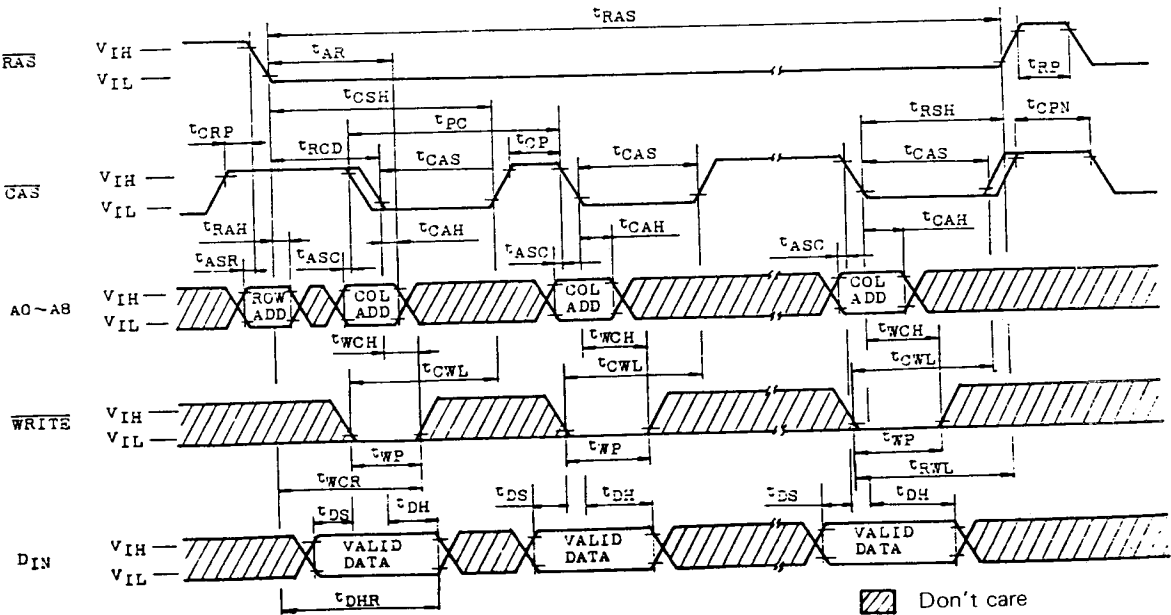


TMM41256AP/AT/AZ-10, TMM41256AP/AT/AZ-12 TMM41256AP/AT/AZ-15

● PAGE MODE READ CYCLE

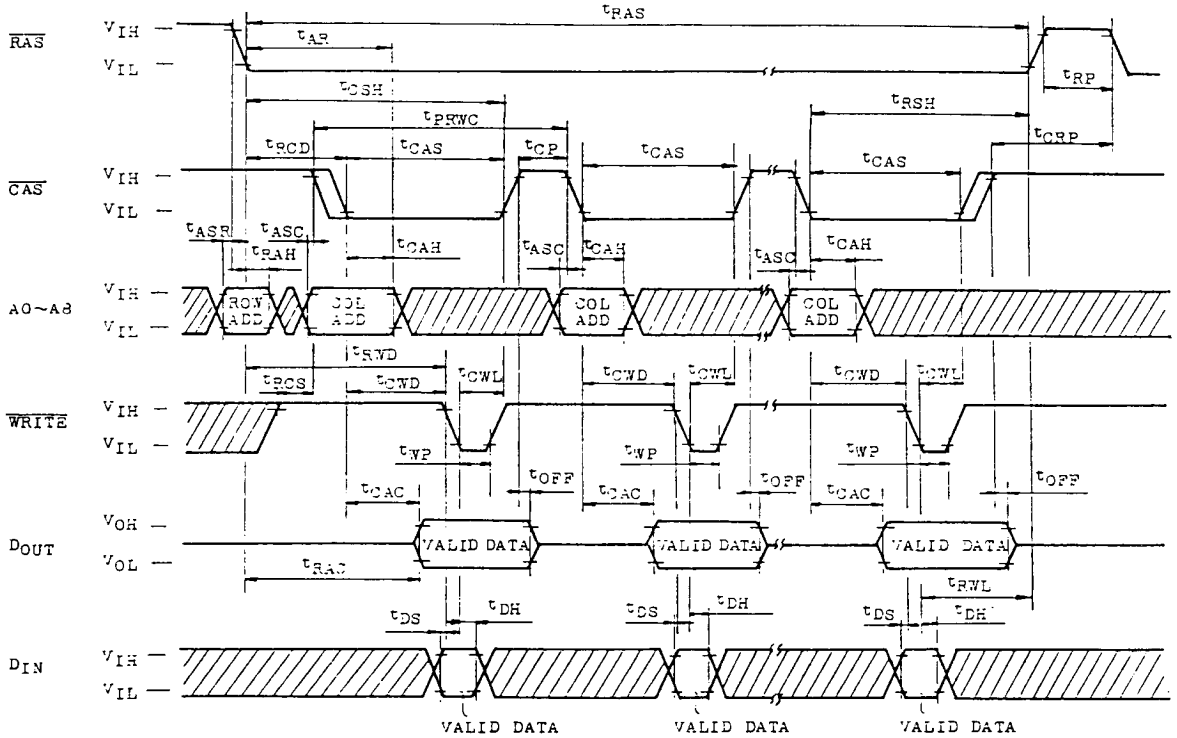



● PAGE MODE WRITE CYCLE (EARLY WRITE)



TMM41256AP/AT/AZ-10, TMM41256AP/AT/AZ-12 TMM41256AP/AT/AZ-15

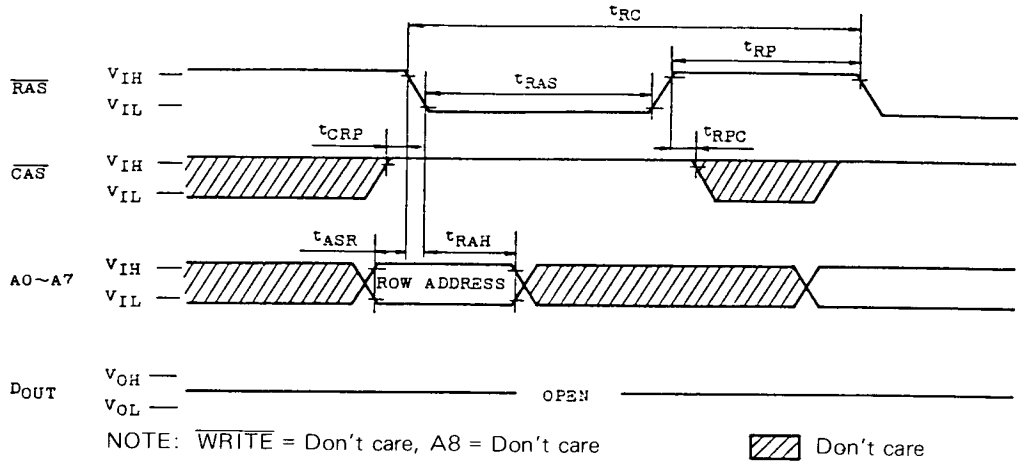
- PAGE MODE READ-WRITE/READ-MODIFY-WRITE CYCLE



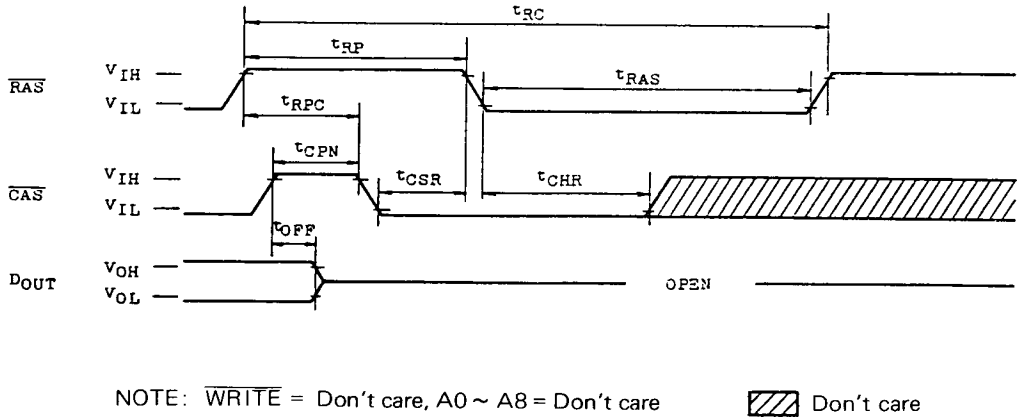
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• $\overline{\text{RAS}}$ ONLY REFRESH CYCLE

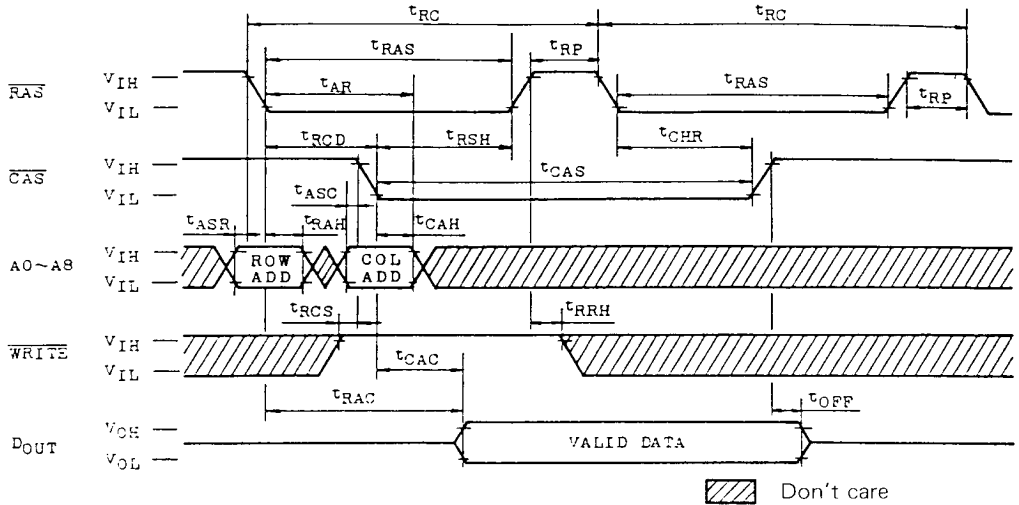


• $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE

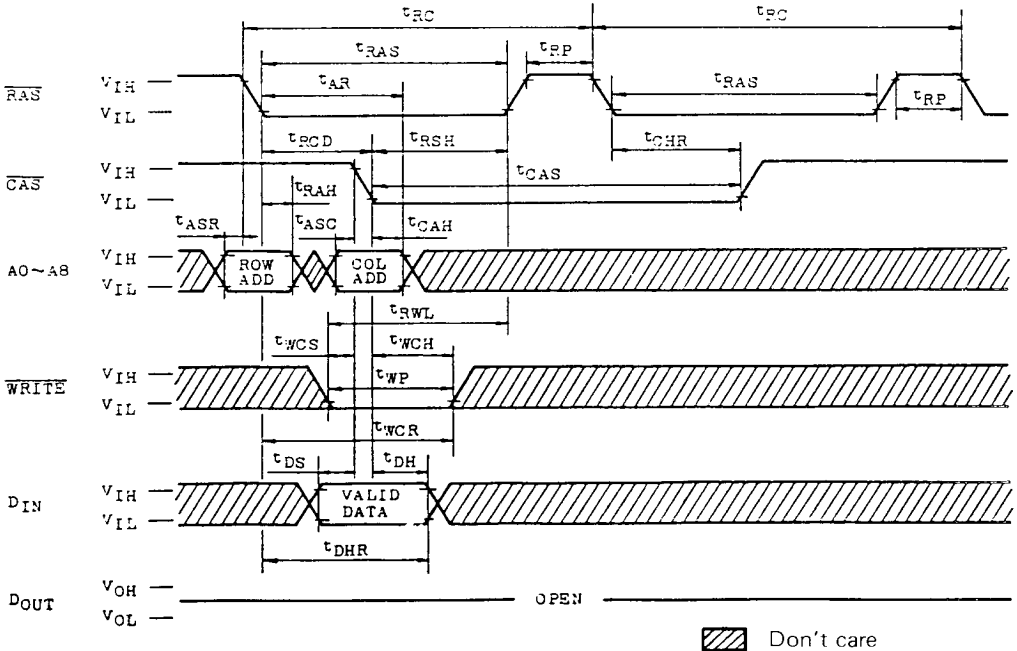


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• HIDDEN REFRESH CYCLE (READ)

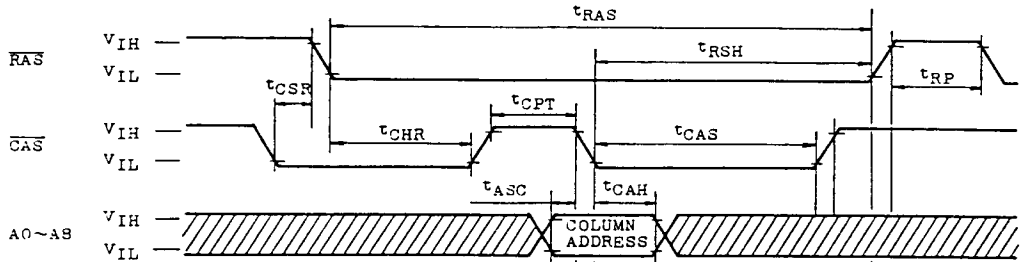


• HIDDEN REFRESH CYCLE (WRITE)

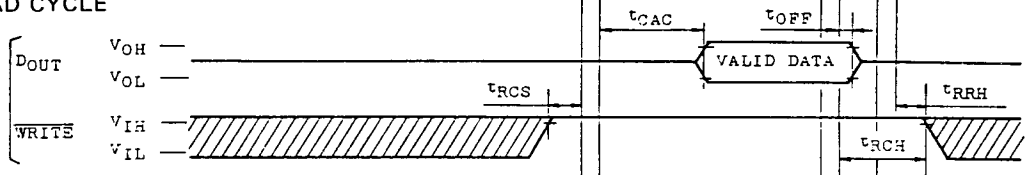


TMM41256AP/AT/AZ-10, TMM41256AP/AT/AZ-12 TMM41256AP/AT/AZ-15

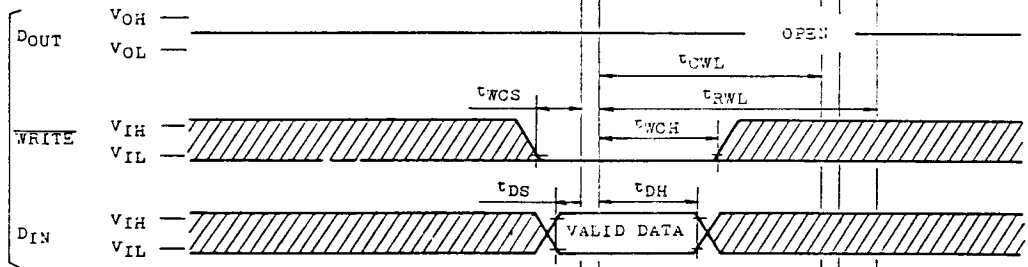
• CAS BEFORE RAS REFRESH COUNTER TEST CYCLE



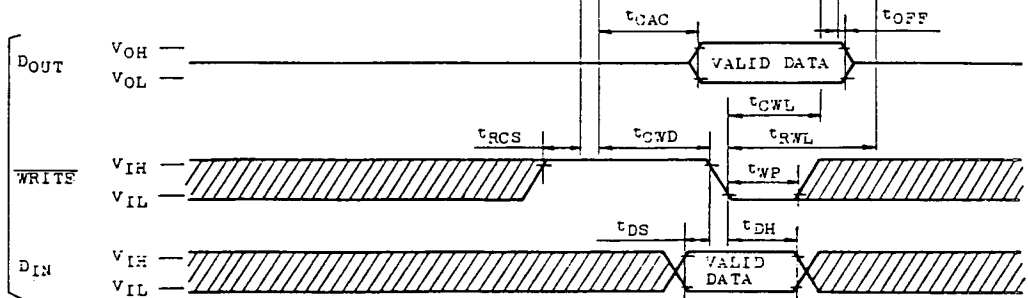
• READ CYCLE



• WRITE CYCLE



• READ-WRITE/READ-MODIFY-WRITE CYCLE



Don't care

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APPLICATION INFORMATION

ADDRESSING

The 18 address bits required to decode 1 of the 262,144 cell locations within the TMM41256AP/AT/AZ are multiplexed onto the 9 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks.

The first clock, the Row Address Strobe ($\overline{\text{RAS}}$), latches the 9 row address bits into the chip. The second clock, the Column Address Strobe ($\overline{\text{CAS}}$), subsequently latches the 9 column address bits into the chip. Each of these signals, $\overline{\text{RAS}}$, and $\overline{\text{CAS}}$, triggers a sequence of events which are controlled by different delayed internal clocks.

The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the $\overline{\text{CAS}}$ clock sequence are inhibited until the occurrence of a delayed signal derived from the $\overline{\text{RAS}}$ clock chain. This "gated $\overline{\text{CAS}}$ " feature allows the $\overline{\text{CAS}}$ clock to be externally activated as soon as the Row address Hold Time specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information.

DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of $\overline{\text{WRITE}}$ and $\overline{\text{CAS}}$ while $\overline{\text{RAS}}$ is active. The later of the signals ($\overline{\text{WRITE}}$ or $\overline{\text{CAS}}$) to make its negative transition is the strobe for the Data In (D_{IN}) register. This permits several options in the write cycle timing. In a write cycle, if the $\overline{\text{WRITE}}$ input is brought low (active) prior to $\overline{\text{CAS}}$, the D_{IN} is strobed by $\overline{\text{CAS}}$ and the set-up and hold times are referenced to $\overline{\text{CAS}}$. If the input data is not available at $\overline{\text{CAS}}$ time or if it is desired that the cycle be a read-write cycle, the $\overline{\text{WRITE}}$ signal will be delayed until after $\overline{\text{CAS}}$ has made its negative transition. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of $\overline{\text{WRITE}}$ rather than $\overline{\text{CAS}}$. (To illustrate this feature, D_{IN} is referenced to $\overline{\text{WRITE}}$ in the timing diagrams depicting the read-write and page mode write cycles while the "early write" cycle diagram shows D_{IN} referenced to $\overline{\text{CAS}}$).

Data is retrieved from the memory in a read cycle by maintaining $\overline{\text{WRITE}}$ in the inactive or high state throughout the portion of the memory cycle in

which $\overline{\text{CAS}}$ is active (low). Data read from the selected cell will be available at the output within the specified access time.

DATA OUTPUT CONTROL

The normal condition of the Data Output (D_{OUT}) of the TMM41256AP/AT/AZ is the high impedance (open circuit) state. This is to say, anytime $\overline{\text{CAS}}$ is at a high level, the D_{OUT} pin will be floating. The only time the output will turn on and contain either a logic 0 or logic 1 is at access time during a read cycle. D_{OUT} will remain valid from access time until $\overline{\text{CAS}}$ is taken back to the inactive (high level) condition.

PAGE MODE

The "Page-Mode" feature of the TMM41256AP/AT/AZ allows for successive memory operations at multiple column locations of the same row address with increased speed without an increase in power. This is done by strobing the row address into the chip and maintaining the $\overline{\text{RAS}}$ signal at a logic 0 throughout all successive memory cycles in which the row address is common. This "Page Mode" of operation will not dissipate the power associated with the negative going edge of $\overline{\text{RAS}}$. Also, the time required for strobing in a new row address is eliminated, thereby decreasing the access and cycle times.

$\overline{\text{RAS}}$ ONLY REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 256 row address ($A_0 \sim A_7$) within each 4 millisecond time interval. Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with " $\overline{\text{RAS}}$ -only" cycles, $\overline{\text{RAS}}$ only refresh results in a substantial reduction in operating power. This reduction in power is reflected in the I_{CC3} specification.

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH

$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refreshing available on the TMM41256AP/AT/AZ offers an alternate refresh method. If $\overline{\text{CAS}}$ is held on low for the specified period (t_{CSR}) before $\overline{\text{RAS}}$ goes to low, on chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed,

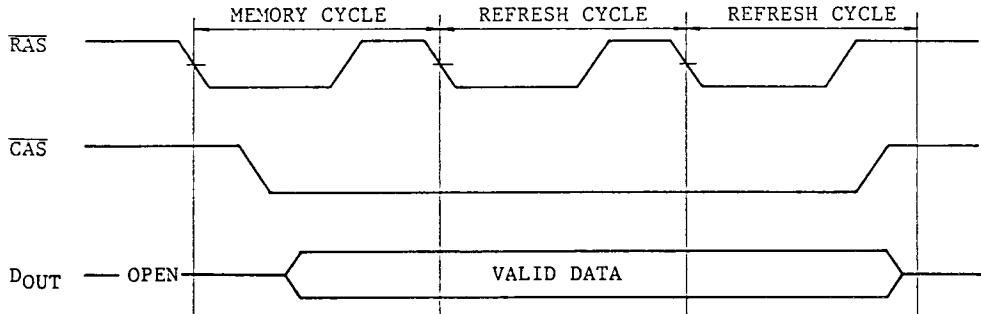
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the refresh address counter is automatically incremented in preparation for the next $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh operation.

HIDDEN REFRESH

An optional feature of the TMM41256AP/AT/AZ

is that refresh cycles may be performed while maintaining valid data at the output pin. This is referred to as Hidden Refresh. Hidden Refresh is performed by holding $\overline{\text{CAS}}$ at V_{IL} and taking $\overline{\text{RAS}}$ high and after a specified precharge period (t_{RP}), executing a $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle. (see Figure below)



This feature allows a refresh cycle to be "hidden" among data cycles without affecting the data availability.

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST

The internal refresh operation of TMM41256AP/AT/AZ can be tested by $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST. This cycle performs READ/WRITE operation taking the internal counter address as row address and the input address as column address.

The test is performed after a minimum of 8 $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ cycles as initialization cycles. The test procedure is as follows.

① Write "0" into all the memory cells at normal

write mode.

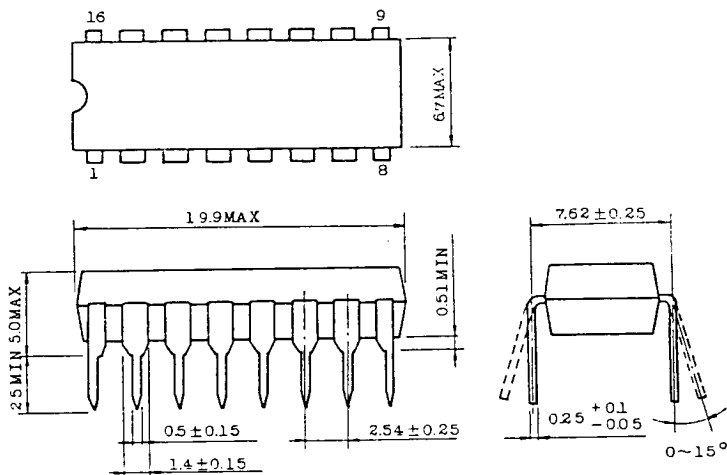
- ② Select one certain column address and read "0" out and write "1" in each cell by performing $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST (READ-WRITE CYCLE). Repeat this operation 256 times.
- ③ Check "1" out of 256 bits at normal read mode, which was written at ②.
- ④ Using the same column as ②, read "1" out and write "0" in each cell performing $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST. Repeat this operation 256 times.
- ⑤ Check "0" out of 256 bits at normal read mode, which was written at ④.
- ⑥ Perform the above ① to ⑤ the complement data.

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OUTLINE DRAWINGS

- Plastic DIP

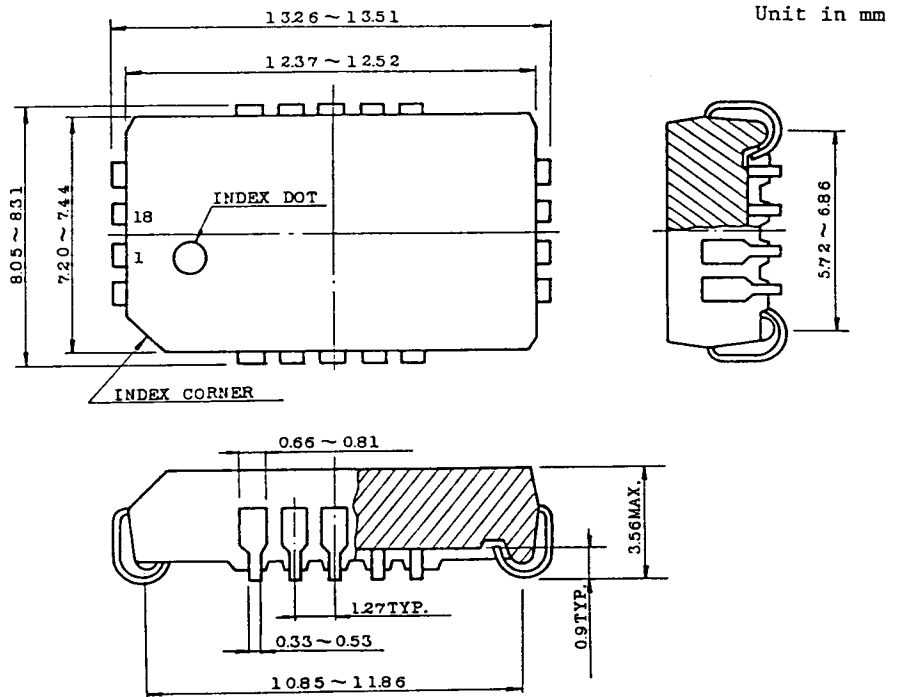
Unit in mm



NOTE: Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No. 1 and No. 16 leads. All dimensions are in millimeters.

TMM41256AP/AT/AZ-10, TMM41256AP/AT/AZ-12 TMM41256AP/AT/AZ-15

- Plastic LCC

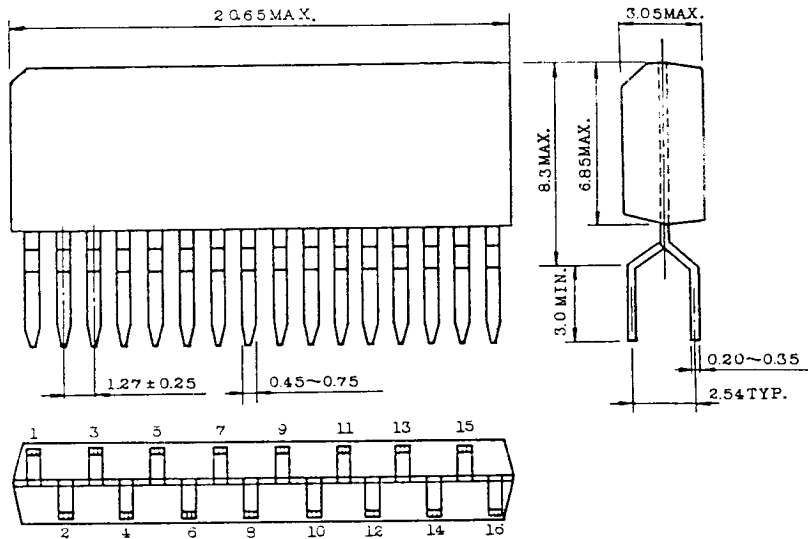


NOTE: Each lead pitch is 1.27mm. All dimensions are in millimeters.

**TMM41256AP/AT/AZ-10, TMM41256AP/AT/AZ-12
TMM41256AP/AT/AZ-15**

- Plastic ZIP

Unit in mm



NOTE: Each lead pitch is 1.27mm. All dimensions are in millimeters.

NOTE: Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.