

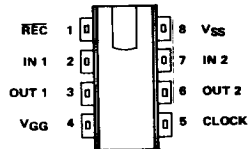
**MOS  
LSI**

**TMS 3126, 3127, 3128, 3129, 3130, 3132 NC  
DUAL 96-, 100-, 128-, 132-, 133-, 133-, 136-, 144-BIT  
STATIC SHIFT REGISTERS**

OCTOBER 1977

- DC to 2.5-MHz Operation
- Static Configuration
- Single TTL-Compatible Clock
- Inputs and Outputs Fully TTL-Compatible
- Push-Pull Output Buffers
- On-Chip Recirculate Logic
- Power Supplies . . . 5 V, -12 V
- Seven Standard Bit Lengths

8-PIN DUAL-IN-LINE PACKAGE  
(TOP VIEW)



**Description**

This series is a family of MOS dual static shift registers. These circuits are monolithically constructed by use of thick-oxide techniques and P-channel enhancement-type transistors, which allow TTL-compatibility for ease of system design.

An on-chip clock generator provides three internal phases from a single external TTL-level clock. All inputs including the low-capacitance clock can be driven directly from Series 74 TTL circuits without the need for pull up resistors. The push-pull outputs are compatible with Series 74 TTL and have a fan-out capability of one TTL load. A current limiter has been incorporated in the output buffers to reduce power dissipation when driving bipolar logic. No external components are needed for TTL interface.

Cross-coupled inverters (flip-flops) are employed to implement each bit storage location. This static design allows input data rates from dc to 2.5 MHz and long-term data storage. Recirculate logic has been incorporated on the chip to simplify system design.

These devices are offered in the 8-pin dual-in-line plastic package (suffix NC). The 8-pin dual-in-line package is designed for insertion in mounting-hole rows on 300-mil centers. These devices are characterized for operation from -25°C to 85°C.

**Applications**

Various bit lengths are offered to cover most computer peripheral applications such as printers, buffer memories, and CRT refresh memories.

**Operation**

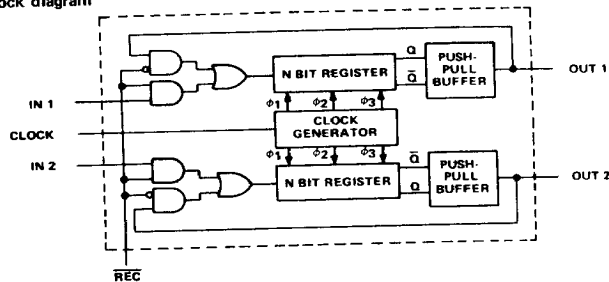
Transfer of data into and out of the shift registers occurs on the low-to-high transition of the clock. Input data must be set up a minimum time before the low-to-high clock transition and must be held for a minimum time after that transition. For long-term data storage, the clock must be maintained high, and in this mode the recirculate and data input levels may change without affecting the data output levels.

Recirculate occurs on the low-to-high clock transition with the recirculate control low. The recirculate control must be set up a minimum time before this transition and held a minimum time after the transition. Data is entered with the recirculate control high. During recirculation, data is continuously available at the output and the data input is inhibited.

SHIFT  
REGISTERS

# TMS 3126, 3127, 3128, 3129, 3130, 3132 NC DUAL 96-, 100-, 128-, 132-, 133-, 133-, 136-, 144-BIT STATIC SHIFT REGISTERS

functional block diagram



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)\***

Supply voltage, $V_{GG}$ (see Note 1)	-20 V to 0.3 V
Clock input voltage (see Note 1)	-20 V to 0.3 V
Data input voltage (see Note 1)	-20 V to 0.3 V
Operating free-air temperature range	-25°C to 85°C
Storage temperature range	-55°C to 150°C

NOTE 1: Under absolute maximum ratings, voltage values are with respect to the normally most-positive supply,  $V_{GG}$  (substrate). Throughout the remainder of this data sheet voltage values are with respect to a floating ground.  
\*Comment: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

**recommended operating conditions**

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, $V_{GG}$	-11	-12	-13	V
Supply voltage, $V_{SS}$	4.5	5	5.5	V
High-level input voltage, $V_{IH}$	$V_{SS} - 1.8$			V
Low-level input voltage, $V_{IL}$			$V_{SS} - 3.9$	V
Clock pulse transition time, low-to-high level, $t_{TLH(\phi)}$			0.02	5 $\mu$ s
Clock pulse transition time, high-to-low level, $t_{THL(\phi)}$			0.02	5 $\mu$ s
Pulse width, clock high, $t_{w(\phi H)}$	300		$\infty$	ns
Pulse width, clock low, $t_{w(\phi L)}$	100		1000000	ns
Recirculate pulse width, $t_{w(rec)}$	125			ns
Data setup time, $t_{su}(da)$	80			ns
Recirculate setup time, $t_{su}(rec)$	100			ns
Data hold time, $t_h(da)$	80			ns
Recirculate hold time, $t_h(rec)$	25			ns
Clock frequency, $f_{\phi}$	0		2.5	MHz
Operating free-air temperature, $T_A$	-25		85	°C

# TMS 3126, 3127, 3128, 3129, 3130, 3132 MC DUAL 96-, 100-, 128-, 132-, 133-, 133-, 136-, 144-BIT STATIC SHIFT REGISTERS

Electrical characteristics under nominal operating conditions,  $T_A = -25^\circ\text{C}$  to  $85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$V_{OH}$	High-level output voltage $I_{OH} = 0.2\text{ mA}$	4			V
$V_{OL}$	Low-level output voltage $I_{OL} = 1.6\text{ mA}$			0.4	V
$I_I$	Input current (all inputs) $V_I = 0.8\text{ V}$		-22	-30	mA
$I_{GG}$	Supply current from $V_{GG}$ $T_A = 25^\circ\text{C}$ , $f = 1\text{ MHz}$		374	510	mW
$P_D$	Power dissipation				
$C_i$	Input capacitance, all inputs except clock $V_I = 5\text{ V}$ , $f = 1\text{ MHz}$		3.5	5	pF
$C_{i(\phi)}$	Clock input capacitance $V_{i(\phi)} = 5\text{ V}$ , $f = 1\text{ MHz}$		3.5	5	pF

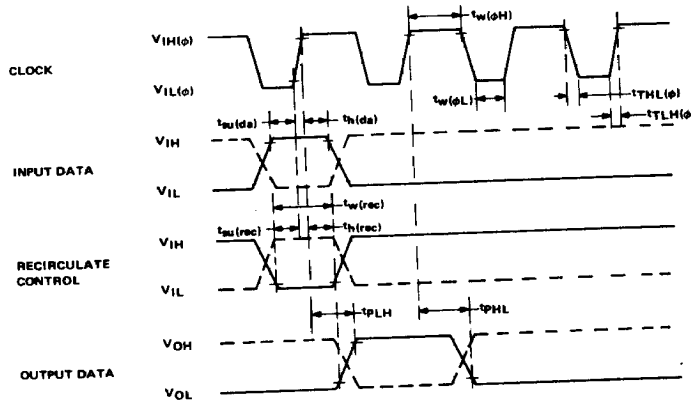
†All typical values are at  $T_A = 25^\circ\text{C}$ .

Switching characteristics under nominal operating conditions,  $T_A = -25^\circ\text{C}$  to  $85^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
$t_{PLH}$	Propagation delay time, low-to-high-level output from clock Load = 1 TTL gate (see Note 2)		250	ns
$t_{PHL}$	Propagation delay time, high-to-low-level output from clock		250	ns

NOTE 2: For test purposes, a TTL load is simulated by a load of 2.7 k $\Omega$  and 20 pF between the output and  $V_{SS}$ .

voltage waveforms



NOTE: All timing measurements are made at 10% or 90% points.

PRINTED IN U.S.A.

TEXAS INSTRUMENTS RESERVES THE RIGHT TO MAKE CHANGES AT ANY TIME TO IMPROVE DESIGN AND TO SUPPLY THE BEST PRODUCT POSSIBLE.

**TEXAS INSTRUMENTS**  
INCORPORATED  
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

181

SHIFT REGISTER