

# TMS4464

## 65,536-WORD BY 4-BIT DYNAMIC RANDOM-ACCESS MEMORY

NOVEMBER 1983 — REVISED JUNE 1987

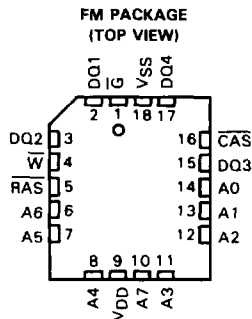
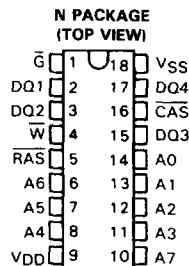
Dynamic RAMs

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- 65,536 × 4 Organization
- Single 5-V Supply (10% Tolerance)
- JEDEC Standardized Pinout
- Pinout Identical to TMS4416 (16K × 4 Dynamic RAM)
- Performance Ranges:

|            | ACCESS<br>TIME<br>ROW | ACCESS<br>TIME<br>COLUMN | READ<br>OR<br>WRITE<br>CYCLE | READ-<br>MODIFY-<br>WRITE<br>CYCLE |
|------------|-----------------------|--------------------------|------------------------------|------------------------------------|
|            | MAX                   | MAX                      | MIN                          | MIN                                |
| TMS4464-10 | 100 ns                | 50 ns                    | 200 ns                       | 270 ns                             |
| TMS4464-12 | 120 ns                | 60 ns                    | 220 ns                       | 295 ns                             |
| TMS4464-15 | 150 ns                | 75 ns                    | 260 ns                       | 345 ns                             |

- Long Refresh Period . . . 4 ms (Max)
- Low Refresh Overhead Time . . . As Low As 1.3% of Total Refresh Period
- On-Chip Substrate Bias Generator
- All Inputs, Outputs, and Clocks Fully TTL Compatible
- 3-State Unlatched Output
- Early Write or  $\overline{G}$  to Control Output Buffer Impedance
- Page-Mode Operation for Faster Access
- Power Dissipation As Low As:
  - Operating . . . 330 mW (Max)
  - Standby . . . 25 mW (Max)
  - (for 150 ns devices)
- $\overline{RAS}$ -Only Refresh Mode
- $\overline{CAS}$ -Before- $\overline{RAS}$  Refresh Mode
- Available with MIL-STD-883C, Class B Processing and S (-55°C to 110°C) Temperature Ranges (SMJ4464)



| PIN NOMENCLATURE |                       |
|------------------|-----------------------|
| A0-A7            | Address Inputs        |
| $\overline{CAS}$ | Column-Address Strobe |
| DQ1-DQ4          | Data In/Data Out      |
| $\overline{G}$   | Output Enable         |
| $\overline{RAS}$ | Row-Address Strobe    |
| VDD              | 5-V Supply            |
| VSS              | Ground                |
| $\overline{W}$   | Write Enable          |

### description

The TMS4464 is a high-speed, 262,144-bit dynamic random-access memory, organized as 65,536 words of four bits each. It employs state-of-the-art SMOS (scaled MOS) N-channel double-level polysilicon/polyicide gate technology for very high performance combined with low cost and improved reliability.

This device features maximum  $\overline{RAS}$  access times of 100 ns, 120 ns, or 150 ns. Power dissipation maximums are 330 mW operating and 25 mW standby for 150-ns devices.

New SMOS technology permits operation from a single 5-V supply, reducing system power supply and decoupling requirements, and easing board layout.  $I_{DD}$  peaks are 125 mA typical, and a -1-V input voltage undershoot can be tolerated, minimizing system noise considerations.

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All inputs and outputs, including clocks, are compatible with Series 74 TTL. All address and data-in lines are latched on chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TMS4464 is offered in 18-pin plastic dual-in-line and 18-lead plastic chip carrier packages. It is guaranteed for operation from 0°C to 70°C. The dual-in-line package is designed for insertion in mounting-hole rows on 7.62-mm (300-mil) centers.

### operation

#### address (A0 through A7)

Sixteen address bits are required to decode 1 of 65,536 storage locations. Eight row-address bits are set up on pins A0 through A7 and latched onto the chip by the row-address strobe ( $\overline{RAS}$ ). Then the eight column-address bits are set up on pins A0 through A7 and latched onto the chip by the column-address strobe ( $\overline{CAS}$ ). All addresses must be stable on or before the falling edges of  $\overline{RAS}$  and  $\overline{CAS}$ .  $\overline{RAS}$  is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder.  $\overline{CAS}$  is used as a chip select activating the column decoder and the input and output buffers.

#### write enable ( $\overline{W}$ )

The read or write mode is selected through the write-enable ( $\overline{W}$ ) input. A logic high on the  $\overline{W}$  input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected. When  $\overline{W}$  goes low prior to  $\overline{CAS}$ , data out will remain in the high-impedance state for the entire cycle permitting common I/O operation.

#### data in (DQ1-DQ4)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling edge of  $\overline{CAS}$  or  $\overline{W}$  strobes data into the on-chip data latches. These latches can be driven from standard TTL circuits without a pull-up resistor. In an early write cycle,  $\overline{W}$  is brought low prior to  $\overline{CAS}$  and the data is strobed in by  $\overline{CAS}$  with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle,  $\overline{CAS}$  will already be low, thus the data will be strobed in by  $\overline{W}$  with setup and hold times referenced to this signal. In a delayed or read-modify-write cycle,  $\overline{G}$  must be high to bring the output buffers to high impedance prior to impressing data on the I/O lines.

#### data out (DQ1-DQ4)

The three-state output buffer provides direct TTL compatibility (no pull-up resistor required) with a fan-out of two Series 74 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until  $\overline{CAS}$  is brought low. In a read cycle the output goes active after the access time interval  $t_{a(C)}$  that begins with the negative transition of  $\overline{CAS}$  as long as  $t_{a(R)}$  and  $t_{a(G)}$  are satisfied. The output becomes valid after the access time has elapsed and remains valid while  $\overline{CAS}$  and  $\overline{G}$  are low.  $\overline{CAS}$  or  $\overline{G}$  going high returns it to a high-impedance state. In a delayed-write or read-modify-write cycle, the output must be put in the high-impedance state prior to applying data to the DQ input. This is accomplished by bringing  $\overline{G}$  high prior to applying data, thus satisfying  $t_{GHD}$ .

#### output enable ( $\overline{G}$ )

The  $\overline{G}$  input controls the impedance of the output buffers. When  $\overline{G}$  is high, the buffers will remain in the high-impedance state. Bringing  $\overline{G}$  low during a normal cycle will activate the output buffers putting them in the low-impedance state. It is necessary for both  $\overline{RAS}$  and  $\overline{CAS}$  to be brought low for the output buffers to go into the low-impedance state. Once in the low-impedance state they will remain in the low-impedance state until  $\overline{G}$  or  $\overline{CAS}$  is brought high.

**refresh**

A refresh operation must be performed at least once every four milliseconds to retain data. This can be achieved by strobing each of the 256 rows (A0-A7). A normal read or write cycle will refresh all bits in each row that is selected. A RAS-only operation can be used by holding  $\overline{\text{CAS}}$  at the high (inactive) level, thus conserving power as the output buffer remains in the high-impedance state.

**$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh**

The  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh is utilized by bringing  $\overline{\text{CAS}}$  low earlier than  $\overline{\text{RAS}}$  (see parameter  $t_{\text{CLRL}}$ ) and holding it low after  $\overline{\text{RAS}}$  falls (see parameter  $t_{\text{RLCHR}}$ ). For successive  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh cycles,  $\overline{\text{CAS}}$  can remain low while cycling  $\overline{\text{RAS}}$ . The external address is ignored and the refresh address is generated internally.

**hidden refresh**

Hidden refresh may be performed while maintaining valid data at the output pin. This is accomplished by holding  $\overline{\text{CAS}}$  at  $V_{\text{IL}}$  after a read operation and cycling  $\overline{\text{RAS}}$  after a specified precharge period, similar to a  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh cycle. The external address is also ignored during the hidden refresh cycles. The data at the output pin remains valid up to the maximum  $\overline{\text{CAS}}$  low pulse duration,  $t_{\text{W}}(\text{CL})$ .

**page mode**

Page-mode operation allows effectively faster memory access by keeping the same row address and strobing random column addresses onto the chip. Thus, the time required to set up and strobe row addresses for the same page is eliminated. The maximum number of columns that can be addressed is determined by  $t_{\text{W}}(\text{RL})$ , the maximum  $\overline{\text{RAS}}$  low pulse duration.

**power up**

To achieve proper device operation, an initial pause of 200  $\mu\text{s}$  is required after power up, followed by a minimum of eight initialization cycles.

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>**

|                                                                            |                |
|----------------------------------------------------------------------------|----------------|
| Voltage on any pin including $V_{\text{DD}}$ supply (see Note 1) . . . . . | -1 V to 7 V    |
| Short circuit output current . . . . .                                     | 50 mA          |
| Power dissipation . . . . .                                                | 1 W            |
| Operating free-air temperature . . . . .                                   | 0°C to 70°C    |
| Storage temperature range . . . . .                                        | -65°C to 150°C |

<sup>†</sup>Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to  $V_{\text{SS}}$ .

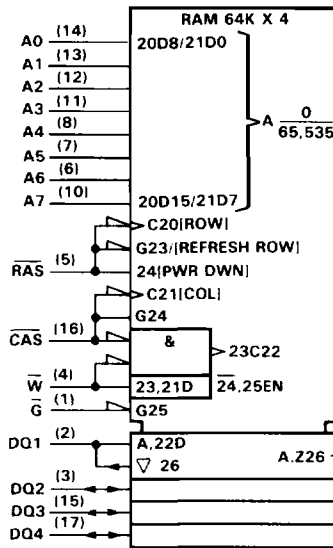
**recommended operating conditions**

|                                                      | MIN | NOM | MAX               | UNIT |
|------------------------------------------------------|-----|-----|-------------------|------|
| $V_{\text{DD}}$ Supply voltage                       | 4.5 | 5   | 5.5               | V    |
| $V_{\text{SS}}$ Supply voltage                       | 0   |     |                   | V    |
| $V_{\text{IH}}$ High-level input voltage             | 2.4 |     | $V_{\text{DD}}+1$ | V    |
| $V_{\text{IL}}$ Low-level input voltage (see Note 2) | -1  |     | 0.8               | V    |
| $T_{\text{A}}$ Operating free-air temperature        | 0   |     | 70                | °C   |

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as maximum, is used in this data sheet for logic voltage levels only.

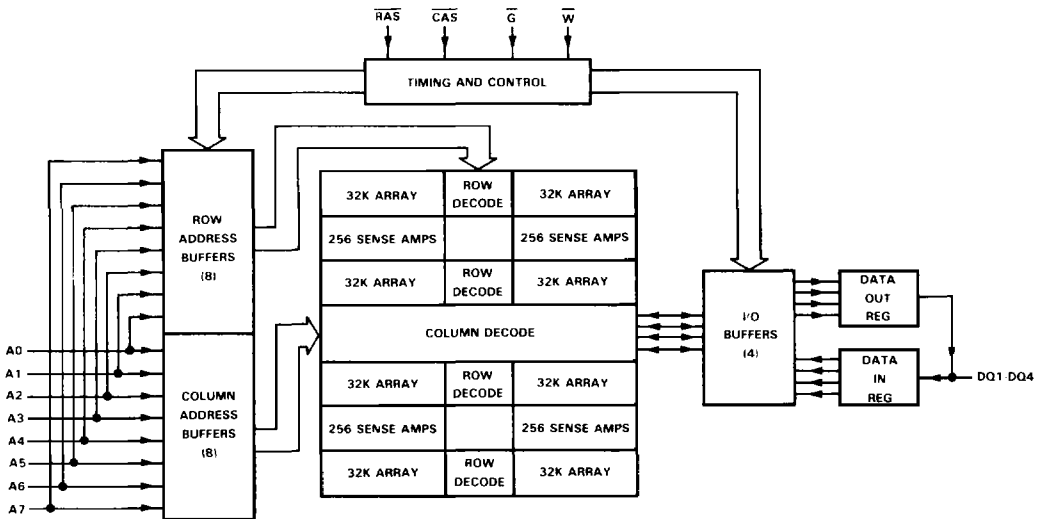
**TMS4464**  
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logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the dual-in-line package.

functional block diagram



**TMS4464**  
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**electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)**

| PARAMETER                                                             | TEST CONDITIONS                                                                                                         | TMS4464-10 |      | TMS4464-12 |      | UNIT |
|-----------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------|------------|------|------------|------|------|
|                                                                       |                                                                                                                         | MIN        | MAX  | MIN        | MAX  |      |
| V <sub>OH</sub> High-level output voltage                             | I <sub>OH</sub> = -5 mA                                                                                                 | 2.4        |      | 2.4        |      | V    |
| V <sub>OL</sub> Low-level output voltage                              | I <sub>OL</sub> = 4.2 mA                                                                                                |            | 0.4  |            | 0.4  | V    |
| I <sub>I</sub> Input current (leakage)                                | V <sub>I</sub> = 0 V to 6.5 V, V <sub>DD</sub> = 5 V, All other pins = 0 V to 6.5 V                                     |            | ± 10 |            | ± 10 | μA   |
| I <sub>O</sub> Output current (leakage)                               | V <sub>O</sub> = 0 V to 5.5 V, V <sub>DD</sub> = 5 V, $\overline{\text{CAS}}$ high, All outputs open                    |            | ± 10 |            | ± 10 | μA   |
| I <sub>DD1</sub> Average operating current during read or write cycle | t <sub>c</sub> = minimum cycle, All outputs open                                                                        |            | 70   |            | 65   | mA   |
| I <sub>DD2</sub> Standby current                                      | After 1 memory cycle, DQ1-DQ4 held at > 0 V, $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ high, All outputs open |            | 4.5  |            | 4.5  | mA   |
| I <sub>DD3</sub> Average refresh current                              | t <sub>c</sub> = minimum cycle, $\overline{\text{RAS}}$ low, $\overline{\text{CAS}}$ high, All outputs open             |            | 58   |            | 53   | mA   |
| I <sub>DD4</sub> Average page-mode current                            | t <sub>c(P)</sub> = minimum cycle, $\overline{\text{RAS}}$ low and $\overline{\text{CAS}}$ cycling, All outputs open    |            | 50   |            | 45   | mA   |

| PARAMETER                                                             | TEST CONDITIONS                                                                                                         | TMS4464-15 |      | UNIT |
|-----------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------|------------|------|------|
|                                                                       |                                                                                                                         | MIN        | MAX  |      |
| V <sub>OH</sub> High-level output voltage                             | I <sub>OH</sub> = -5 mA                                                                                                 | 2.4        |      | V    |
| V <sub>OL</sub> Low-level output voltage                              | I <sub>OL</sub> = 4.2 mA                                                                                                |            | 0.4  | V    |
| I <sub>I</sub> Input current (leakage)                                | V <sub>I</sub> = 0 V to 6.5 V, V <sub>DD</sub> = 5 V, All other pins = 0 V to 6.5 V                                     |            | ± 10 | μA   |
| I <sub>O</sub> Output current (leakage)                               | V <sub>O</sub> = 0 V to 5.5 V, V <sub>DD</sub> = 5 V, $\overline{\text{CAS}}$ high, All outputs open                    |            | ± 10 | μA   |
| I <sub>DD1</sub> Average operating current during read or write cycle | t <sub>c</sub> = minimum cycle, All outputs open                                                                        |            | 60   | mA   |
| I <sub>DD2</sub> Standby current                                      | After 1 memory cycle, DQ1-DQ4 held at > 0 V, $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ high, All outputs open |            | 4.5  | mA   |
| I <sub>DD3</sub> Average refresh current                              | t <sub>c</sub> = minimum cycle, $\overline{\text{RAS}}$ low, $\overline{\text{CAS}}$ high, All outputs open             |            | 48   | mA   |
| I <sub>DD4</sub> Average page-mode current                            | t <sub>c(P)</sub> = minimum cycle, $\overline{\text{RAS}}$ low, $\overline{\text{CAS}}$ cycling, All outputs open       |            | 40   | mA   |

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capacitance over recommended supply voltage range and operating free-air temperature range,  
 $f = 1 \text{ MHz}$

| PARAMETER   |                                       | TMS4464 |     | UNIT |
|-------------|---------------------------------------|---------|-----|------|
|             |                                       | MIN     | MAX |      |
| $C_{i(A)}$  | Input capacitance, address inputs     |         | 5   | pF   |
| $C_{i(RC)}$ | Input capacitance, strobe inputs      |         | 7   | pF   |
| $C_{i(W)}$  | Input capacitance, write enable input |         | 7   | pF   |
| $C_{i,o}$   | Output capacitance                    |         | 7   | pF   |

switching characteristics over recommended supply voltage range and operating free-air temperature range

| PARAMETER          | TEST CONDITIONS                                                                 | ALT. SYMBOL | TMS4464-10 |     | TMS4464-12 |     | UNIT |
|--------------------|---------------------------------------------------------------------------------|-------------|------------|-----|------------|-----|------|
|                    |                                                                                 |             | MIN        | MAX | MIN        | MAX |      |
| $t_{a(C)}$         | Access time from $\overline{CAS}$<br>Load = 2 Series 74 TTL gates               | $t_{CAC}$   |            | 50  |            | 60  | ns   |
| $t_{a(R)}$         | Access time from $\overline{RAS}$<br>Load = 2 Series 74 TTL gates               | $t_{RAC}$   |            | 100 |            | 120 | ns   |
| $t_{a(G)}^\dagger$ | Access time after $\overline{G}$ low<br>Load = 2 Series 74 TTL gates            | $t_{GAC}$   |            | 30  |            | 35  | ns   |
| $t_{dis(CH)}$      | Output disable time after $\overline{CAS}$ high<br>Load = 2 Series 74 TTL gates | $t_{OFF}$   | 0          | 30  | 0          | 30  | ns   |
| $t_{dis(G)}$       | Output disable time after $\overline{G}$ high<br>Load = 2 Series 74 TTL gates   | $t_{GOFF}$  | 0          | 30  | 0          | 30  | ns   |

| PARAMETER          | TEST CONDITIONS                                                                       | ALT. SYMBOL | TMS4464-15 |     | UNIT |
|--------------------|---------------------------------------------------------------------------------------|-------------|------------|-----|------|
|                    |                                                                                       |             | MIN        | MAX |      |
| $t_{a(C)}$         | $t_{RLCL} \geq \text{MAX}$ , $C_L = 100 \text{ pF}$ ,<br>Load = 2 Series 74 TTL gates | $t_{CAC}$   |            | 75  | ns   |
| $t_{a(R)}$         | $t_{RLCL} = \text{MAX}$ , $C_L = 100 \text{ pF}$ ,<br>Load = 2 Series 74 TTL gates    | $t_{RAC}$   |            | 150 | ns   |
| $t_{a(G)}^\dagger$ | $C_L = 100 \text{ pF}$ ,<br>Load = 2 Series 74 TTL gates                              | $t_{GAC}$   |            | 40  | ns   |
| $t_{dis(CH)}$      | $C_L = 100 \text{ pF}$ ,<br>Load = 2 Series 74 TTL gates                              | $t_{OFF}$   | 0          | 30  | ns   |
| $t_{dis(G)}$       | $C_L = 100 \text{ pF}$ ,<br>Load = 2 Series 74 TTL gates                              | $t_{GOFF}$  | 0          | 30  | ns   |

$t_{a(C)}$  and  $t_{a(R)}$  must be satisfied to guarantee  $t_{a(G)}$ .

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**timing requirements over recommended supply voltage range and operating free-air temperature range (see Note 3)**

|                                                                                  | ALT. SYMBOL | TMS4464-10 |        | TMS4464-12 |        | UNIT |
|----------------------------------------------------------------------------------|-------------|------------|--------|------------|--------|------|
|                                                                                  |             | MIN        | MAX    | MIN        | MAX    |      |
| $t_c(P)$ Page-mode cycle time                                                    | $t_{PC}$    | 100        |        | 120        |        | ns   |
| $t_c(PM)$ Page-mode cycle time (read-modify-write cycle)                         | $t_{PCM}$   | 170        |        | 195        |        | ns   |
| $t_c(rd)$ Read cycle time <sup>†</sup>                                           | $t_{RC}$    | 200        |        | 220        |        | ns   |
| $t_c(W)$ Write cycle time                                                        | $t_{WC}$    | 200        |        | 220        |        | ns   |
| $t_c(rdW)$ Read-write/read-modify-write cycle time                               | $t_{RW}$    | 270        |        | 295        |        | ns   |
| $t_w(CH)P$ Pulse duration, $\overline{CAS}$ high (page mode)                     | $t_{CP}$    | 40         |        | 50         |        | ns   |
| $t_w(CH)$ Pulse duration, $\overline{CAS}$ high (non-page mode)                  | $t_{CPN}$   | 25         |        | 25         |        | ns   |
| $t_w(CL)$ Pulse duration, $\overline{CAS}$ low <sup>†</sup>                      | $t_{CAS}$   | 50         | 10,000 | 60         | 10,000 | ns   |
| $t_w(RH)$ Pulse duration, $\overline{RAS}$ high                                  | $t_{RP}$    | 90         |        | 90         |        | ns   |
| $t_w(RL)$ Pulse duration, $\overline{RAS}$ low <sup>‡</sup>                      | $t_{RAS}$   | 100        | 10,000 | 120        | 10,000 | ns   |
| $t_w(W)$ Write pulse duration                                                    | $t_{WP}$    | 30         |        | 30         |        | ns   |
| $t_t$ Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$ | $t_T$       | 3          | 50     | 3          | 50     | ns   |
| $t_{su}(CA)$ Column-address setup time                                           | $t_{ASC}$   | 0          |        | 0          |        | ns   |
| $t_{su}(RA)$ Row-address setup time                                              | $t_{ASR}$   | 0          |        | 0          |        | ns   |
| $t_{su}(D)$ Data setup time                                                      | $t_{DS}$    | 0          |        | 0          |        | ns   |
| $t_{su}(rd)$ Read-command setup time                                             | $t_{RCS}$   | 0          |        | 0          |        | ns   |
| $t_{su}(WCL)$ Early write-command setup time before $\overline{CAS}$ low         | $t_{WCS}$   | 0          |        | 0          |        | ns   |
| $t_{su}(WCH)$ Write-command setup time before $\overline{CAS}$ high              | $t_{CWL}$   | 30         |        | 35         |        | ns   |
| $t_{su}(WRH)$ Write-command setup time before $\overline{RAS}$ high              | $t_{RWL}$   | 30         |        | 35         |        | ns   |
| $t_h(CLCA)$ Column-address hold time after $\overline{CAS}$ low                  | $t_{CAH}$   | 15         |        | 20         |        | ns   |
| $t_h(RA)$ Row-address hold time                                                  | $t_{RAH}$   | 15         |        | 15         |        | ns   |
| $t_h(RLCA)$ Column-address hold time after $\overline{RAS}$ low                  | $t_{AR}$    | 65         |        | 80         |        | ns   |
| $t_h(CLD)$ Data hold time after $\overline{CAS}$ low                             | $t_{DH}$    | 30         |        | 30         |        | ns   |
| $t_h(RLD)$ Data hold time after $\overline{RAS}$ low                             | $t_{DHR}$   | 80         |        | 90         |        | ns   |
| $t_h(WLD)$ Data hold time after $\overline{W}$ low                               | $t_{DH}$    | 30         |        | 30         |        | ns   |
| $t_h(CHrd)$ Read-command hold time after $\overline{CAS}$ high                   | $t_{RCH}$   | 0          |        | 0          |        | ns   |
| $t_h(RHrd)$ Read-command hold time after $\overline{RAS}$ high                   | $t_{RRH}$   | 10         |        | 10         |        | ns   |
| $t_h(CLW)$ Write-command hold time after $\overline{CAS}$ low                    | $t_{WCH}$   | 30         |        | 30         |        | ns   |
| $t_h(RLW)$ Write-command hold time after $\overline{RAS}$ low                    | $t_{WCR}$   | 80         |        | 90         |        | ns   |

Continued next page.

NOTE 3: Timing measurements are referenced to  $V_{IL}$  MAX and  $V_{IH}$  MIN.

<sup>†</sup>All cycle times assume  $t_t = 5$  ns.

<sup>†</sup>In a read-modify-write cycle,  $t_{CLWL}$  and  $t_{su}(WCH)$  must be observed. Depending on the user's transition times, this may require additional  $\overline{CAS}$  low time ( $t_{w}(CL)$ ).

<sup>‡</sup>In a read-modify-write cycle,  $t_{RLWL}$  and  $t_{su}(WRH)$  must be observed. Depending on the user's transition times, this may require additional  $\overline{RAS}$  low time ( $t_{w}(RL)$ ).

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timing requirements over recommended supply voltage range and operating free-air temperature range (continued) (see Note 3)

|                                                                                                                                    | ALT. SYMBOL      | TMS4464-10 |     | TMS4464-12 |     | UNIT |
|------------------------------------------------------------------------------------------------------------------------------------|------------------|------------|-----|------------|-----|------|
|                                                                                                                                    |                  | MIN        | MAX | MIN        | MAX |      |
| t <sub>RLCHR</sub> Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high <sup>¶</sup>                                          | t <sub>CHR</sub> | 20         |     | 25         |     | ns   |
| t <sub>RLCH</sub> Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high                                                        | t <sub>CSH</sub> | 100        |     | 120        |     | ns   |
| t <sub>CHRL</sub> Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low                                                        | t <sub>CRP</sub> | 0          |     | 0          |     | ns   |
| t <sub>RHCL</sub> Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low <sup>¶</sup>                                           | t <sub>RPC</sub> | 0          |     | 0          |     | ns   |
| t <sub>CLRH</sub> Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high                                                        | t <sub>RSH</sub> | 50         |     | 60         |     | ns   |
| t <sub>CLWL</sub> Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-modify-write cycle only) <sup>#</sup>               | t <sub>CWD</sub> | 85         |     | 95         |     | ns   |
| t <sub>CLRL</sub> Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low <sup>¶</sup>                                            | t <sub>CSR</sub> | 10         |     | 10         |     | ns   |
| t <sub>RLCL</sub> Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time) | t <sub>RCD</sub> | 25         | 50  | 25         | 60  | ns   |
| t <sub>RLWL</sub> Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-modify-write cycle only) <sup>#</sup>               | t <sub>RWD</sub> | 135        |     | 155        |     | ns   |
| t <sub>GHD</sub> Delay time, $\overline{G}$ high before data applied at DQ                                                         | t <sub>GDD</sub> | 30         |     | 30         |     | ns   |
| t <sub>rf</sub> Refresh time interval                                                                                              | t <sub>REF</sub> |            | 4   |            | 4   | ms   |

NOTE 3: Timing measurements are referenced to V<sub>IL</sub> MAX and V<sub>IH</sub> MIN.

<sup>¶</sup>  $\overline{CAS}$  before  $\overline{RAS}$  refresh option only.

<sup>#</sup>  $\overline{G}$  must disable the output buffers prior to applying data to the device.



**TMS4464**  
**65,536-WORD BY 4-BIT DYNAMIC RANDOM-ACCESS MEMORY**

**timing requirements over recommended supply voltage range and operating free-air temperature range (continued) (see note 3)**

|                                                                                  | ALT. SYMBOL | TMS4464-15 |        | UNIT |
|----------------------------------------------------------------------------------|-------------|------------|--------|------|
|                                                                                  |             | MIN        | MAX    |      |
| $t_{c(P)}$ Page-mode cycle time                                                  | $t_{PC}$    | 145        |        | ns   |
| $t_{c(PM)}$ Page-mode cycle time (read-modify-write cycle)                       | $t_{PCM}$   | 230        |        | ns   |
| $t_{c(rd)}$ Read cycle time <sup>1</sup>                                         | $t_{RC}$    | 260        |        | ns   |
| $t_{c(W)}$ Write cycle time                                                      | $t_{WC}$    | 260        |        | ns   |
| $t_{c(rdW)}$ Read-write/read-modify-write cycle time                             | $t_{RWC}$   | 345        |        | ns   |
| $t_{w(CH)P}$ Pulse duration, $\overline{CAS}$ high (page mode)                   | $t_{CP}$    | 60         |        | ns   |
| $t_{w(CH)}$ Pulse duration, $\overline{CAS}$ high (non-page mode)                | $t_{CPN}$   | 25         |        | ns   |
| $t_{w(CL)}$ Pulse duration, $\overline{CAS}$ low <sup>2</sup>                    | $t_{CAS}$   | 75         | 10,000 | ns   |
| $t_{w(RH)}$ Pulse duration, $\overline{RAS}$ high                                | $t_{RP}$    | 100        |        | ns   |
| $t_{w(RL)}$ Pulse duration, $\overline{RAS}$ low <sup>3</sup>                    | $t_{RAS}$   | 150        | 10,000 | ns   |
| $t_{w(W)}$ Write pulse duration                                                  | $t_{WP}$    | 45         |        | ns   |
| $t_t$ Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$ | $t_T$       | 3          | 50     | ns   |
| $t_{su(CA)}$ Column-address setup time                                           | $t_{ASC}$   | 0          |        | ns   |
| $t_{su(RA)}$ Row-address setup time                                              | $t_{ASR}$   | 0          |        | ns   |
| $t_{su(D)}$ Data setup time                                                      | $t_{DS}$    | 0          |        | ns   |
| $t_{su(rd)}$ Read-command setup time                                             | $t_{RCS}$   | 0          |        | ns   |
| $t_{su(WCL)}$ Early write-command setup time before $\overline{CAS}$ low         | $t_{WCS}$   | 0          |        | ns   |
| $t_{su(WCH)}$ Write-command setup time before $\overline{CAS}$ high              | $t_{CWL}$   | 45         |        | ns   |
| $t_{su(WRH)}$ Write-command setup time before $\overline{RAS}$ high              | $t_{RWL}$   | 45         |        | ns   |
| $t_h(CLCA)$ Column-address hold time after $\overline{CAS}$ low                  | $t_{CAH}$   | 25         |        | ns   |
| $t_h(RA)$ Row-address hold time                                                  | $t_{RAH}$   | 15         |        | ns   |
| $t_h(RLCA)$ Column-address hold time after $\overline{RAS}$ low                  | $t_{AR}$    | 100        |        | ns   |
| $t_h(CLD)$ Data hold time after $\overline{CAS}$ low                             | $t_{DH}$    | 45         |        | ns   |
| $t_h(RLD)$ Data hold time after $\overline{RAS}$ low                             | $t_{DHR}$   | 120        |        | ns   |
| $t_h(WLD)$ Data hold time after $\overline{W}$ low                               | $t_{DH}$    | 45         |        | ns   |
| $t_h(CHrd)$ Read-command hold time after $\overline{CAS}$ high                   | $t_{RCH}$   | 0          |        | ns   |
| $t_h(RHrd)$ Read-command hold time after $\overline{RAS}$ high                   | $t_{RRH}$   | 10         |        | ns   |
| $t_h(CLW)$ Write-command hold time after $\overline{CAS}$ low                    | $t_{WCH}$   | 45         |        | ns   |
| $t_h(RLW)$ Write-command hold time after $\overline{RAS}$ low                    | $t_{WCR}$   | 120        |        | ns   |

Continued next page.

NOTE 3: Timing measurements are referenced to  $V_{IL}$  MAX and  $V_{IH}$  MIN.

<sup>1</sup>All cycle times assume  $t_t = 5$  ns

<sup>2</sup>In a read-modify-write cycle,  $t_{CLWL}$  and  $t_{su(WCH)}$  must be observed. Depending on the user's transition times, this may require additional  $\overline{CAS}$  low time ( $t_{w(CL)}$ ).

<sup>3</sup>In a read-modify-write cycle,  $t_{RLWL}$  and  $t_{su(WRH)}$  must be observed. Depending on the user's transition times, this may require additional  $\overline{RAS}$  low time ( $t_{w(RL)}$ ).

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timing requirements over recommended supply voltage range and operating free-air temperature range (concluded) (see Note 3)

|                                                                                                                                    | ALT. SYMBOL      | TMS4464-15 |     | UNIT |
|------------------------------------------------------------------------------------------------------------------------------------|------------------|------------|-----|------|
|                                                                                                                                    |                  | MIN        | MAX |      |
| t <sub>RLCHR</sub> Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high <sup>†</sup>                                          | t <sub>CHR</sub> | 30         |     | ns   |
| t <sub>RLCH</sub> Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high                                                        | t <sub>CSH</sub> | 150        |     | ns   |
| t <sub>CHRL</sub> Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low                                                        | t <sub>CRP</sub> | 0          |     | ns   |
| t <sub>RHCL</sub> Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low <sup>†</sup>                                           | t <sub>RPC</sub> | 0          |     | ns   |
| t <sub>CLRH</sub> Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high                                                        | t <sub>RSH</sub> | 75         |     | ns   |
| t <sub>CLWL</sub> Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-modify-write cycle only) <sup>#</sup>               | t <sub>CWD</sub> | 110        |     | ns   |
| t <sub>CLRL</sub> Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low <sup>†</sup>                                            | t <sub>CSR</sub> | 20         |     | ns   |
| t <sub>RLCL</sub> Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time) | t <sub>RCD</sub> | 25         | 75  | ns   |
| t <sub>RLWL</sub> Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-modify-write cycle only) <sup>#</sup>               | t <sub>RWD</sub> | 185        |     | ns   |
| t <sub>GHD</sub> Delay time, $\overline{G}$ high before data applied at DQ                                                         | t <sub>GDD</sub> | 30         |     | ns   |
| t <sub>rf</sub> Refresh time interval                                                                                              | t <sub>REF</sub> |            | 4   | ms   |

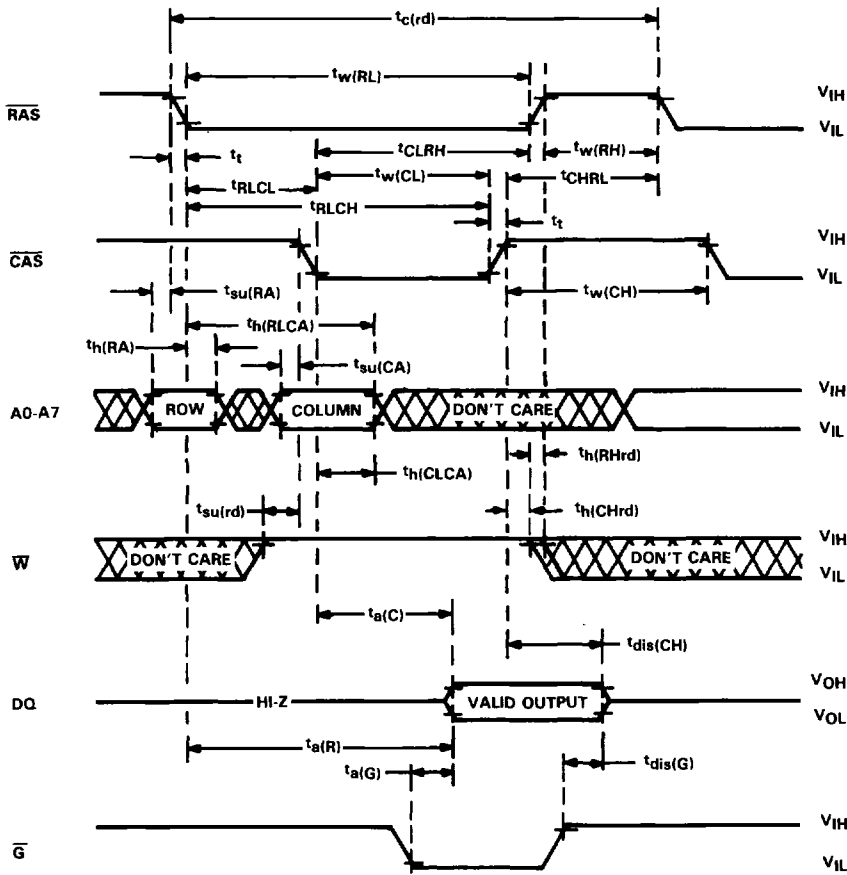
NOTE 3: Timing measurements are referenced to V<sub>IL</sub> MAX and V<sub>IH</sub> MIN.

<sup>†</sup>  $\overline{CAS}$ -before- $\overline{RAS}$  refresh option only.

<sup>#</sup>  $\overline{G}$  must disable the output buffers prior to applying data to the device.

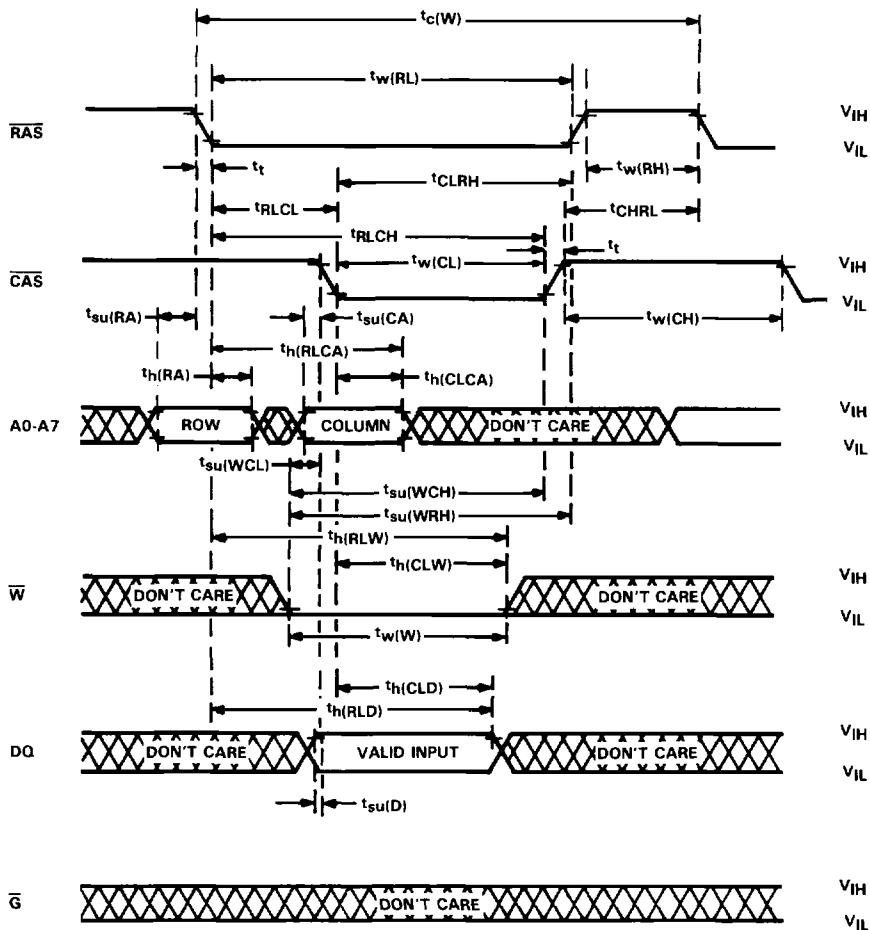
**TMS4464**  
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read cycle timing

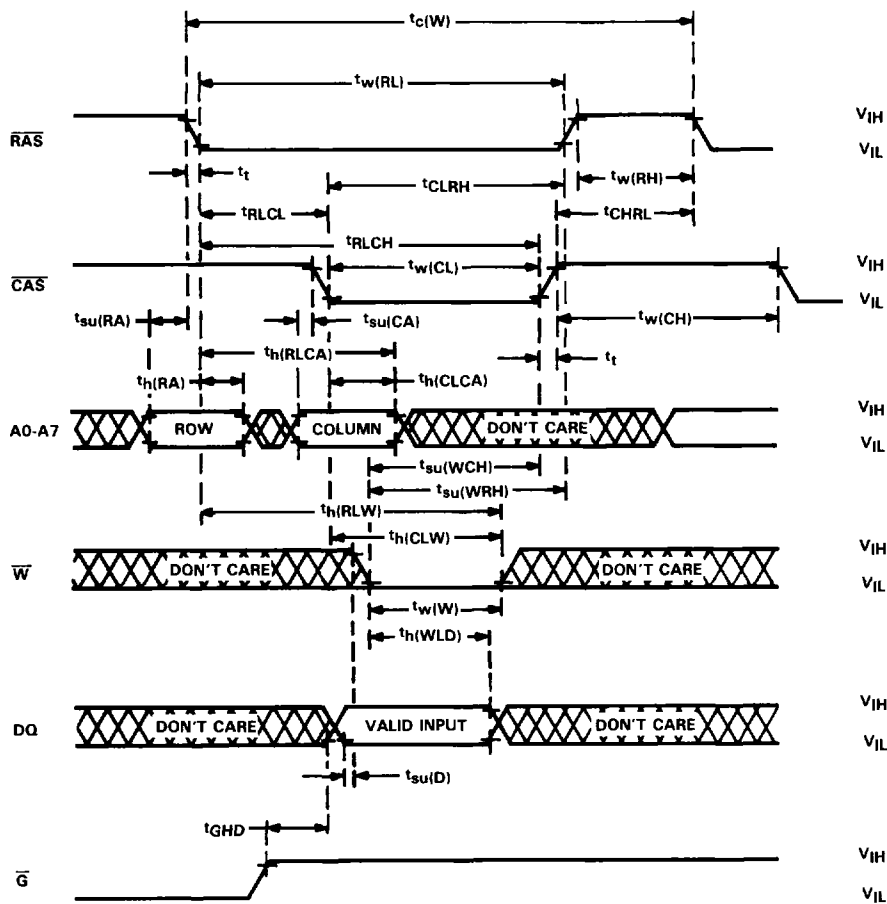


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early write cycle timing



write cycle timing

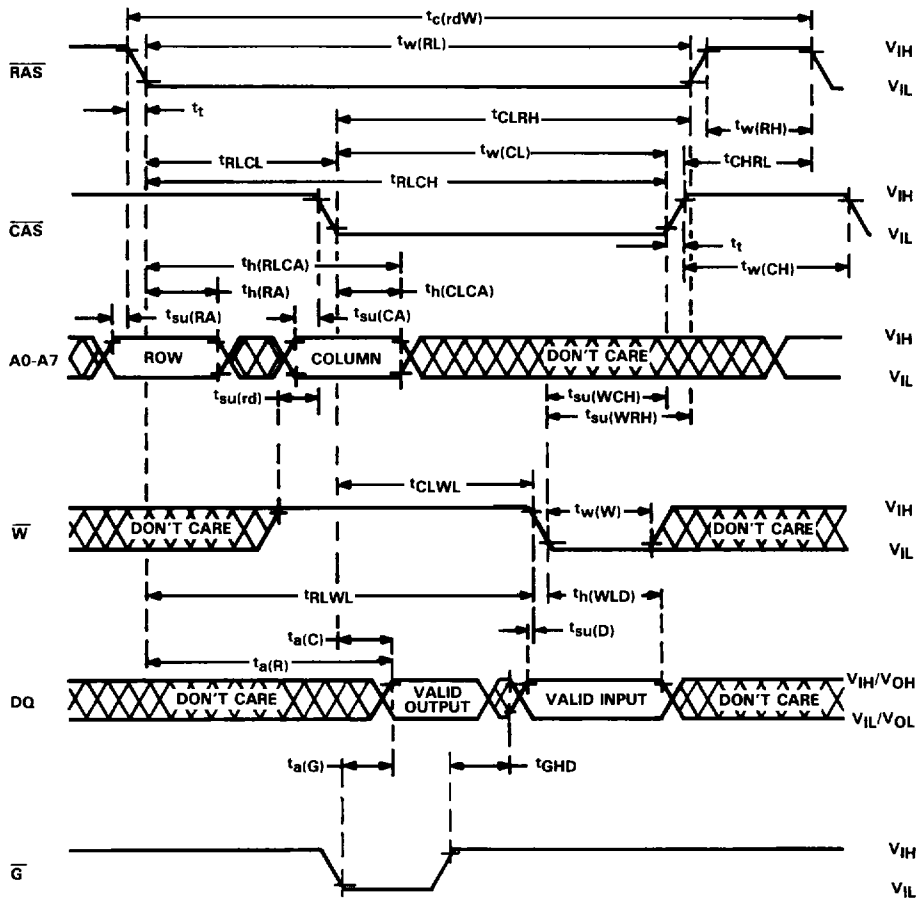


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read-write/read-modify-write cycle timing



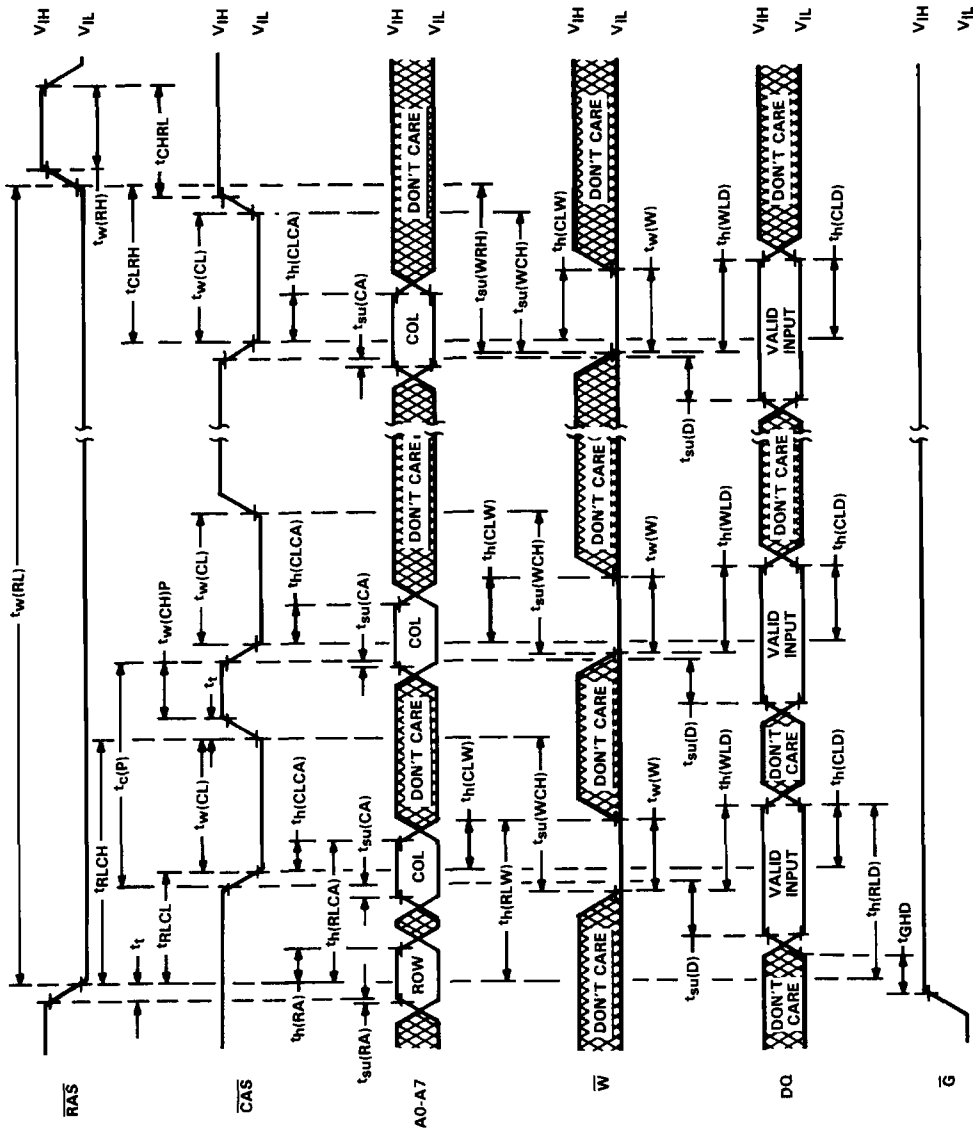


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page-mode write cycle timing

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NOTE 5: A write cycle or read modify write cycle can be intermixed with write cycles as long as the read and read-modify-write timing specifications are not violated.



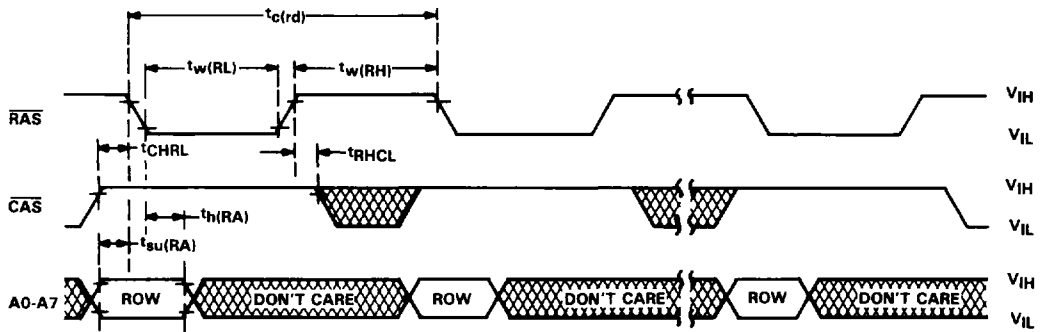


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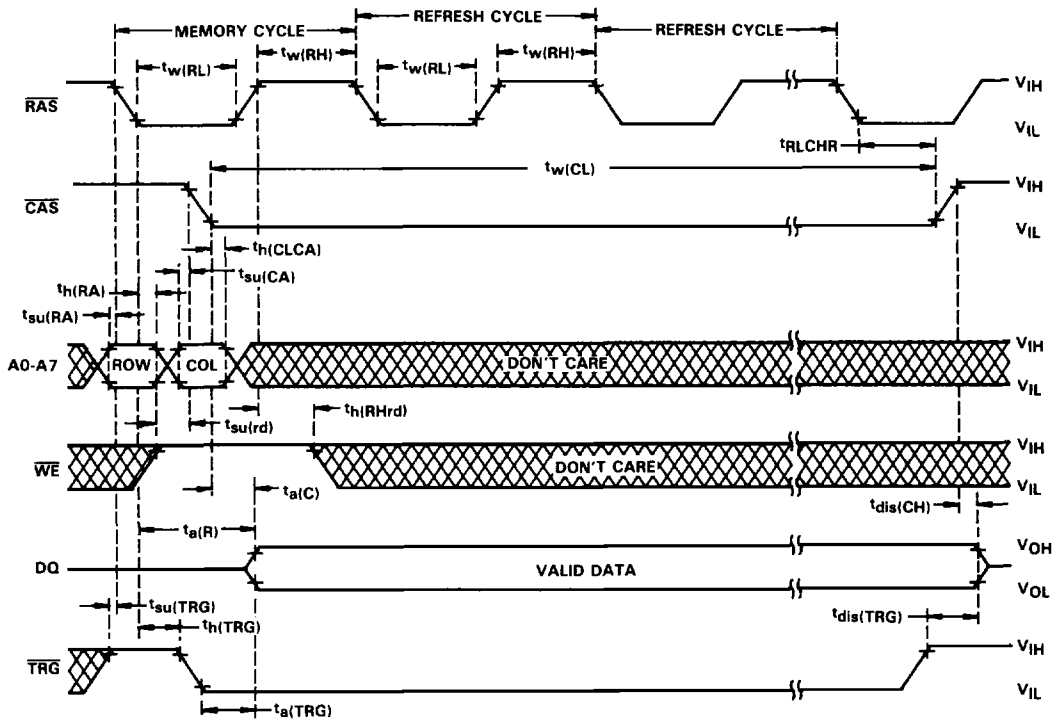
Dynamic RAMs

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**RAS-only refresh cycle timing**



**hidden refresh cycle timing**



$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh cycle timing

