TELEFUNKEN ELECTRONIC

U 6055 B · U 6056 B

MICROCOMPUTER CONTROLLED LOCAL MULTIPLEX SYSTEM

Technology: Bipolar

T-75-45-07

Application:

Transmitter (U 6055 B) and receiver (U 6056 B) for "parallel-serial-parallel"-conversion of a 8 or 16 bit data word via a single data line, working as µP-interfaces.

Features:

- 8/16 bit parallel-serial-parallel conversion
- Only a single data line is necessary
- Quadruple comparison of the data signal for high transmission safety
- Minimum of peripherals
- All output memories are reset if data line is disturbed
- Disturbed data line is displayed
- Transmitter and receiver prepared for master/slave operation
- Transmitter data output short circuit protected
- Transmitter can be powered via data line
- Wide supply voltage range
- Meet the demands of VDE regulation 0839
- Load dump protected

Cases:

14 pin dual inline plastic (U 6055 B, U 6056 B)
16 pin SO plastic (U 6055 B-FP)
20 pin SO plastic (U 6056 B-FP)

T1.2/2113.0690 E

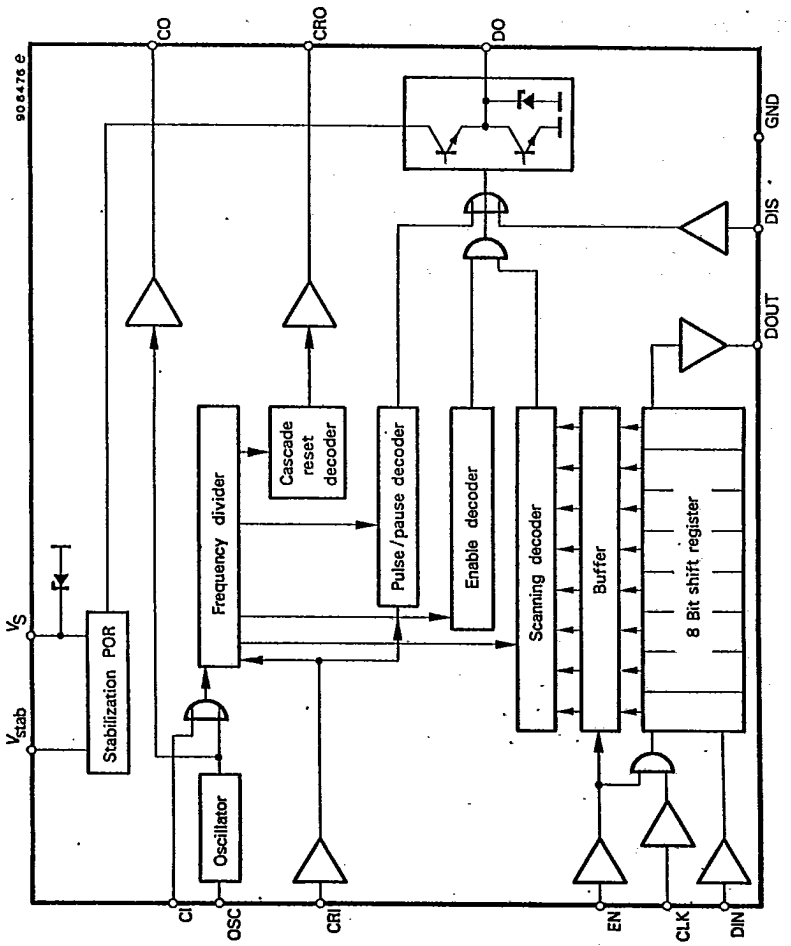

Fig. 1 Block diagram U 6055 B

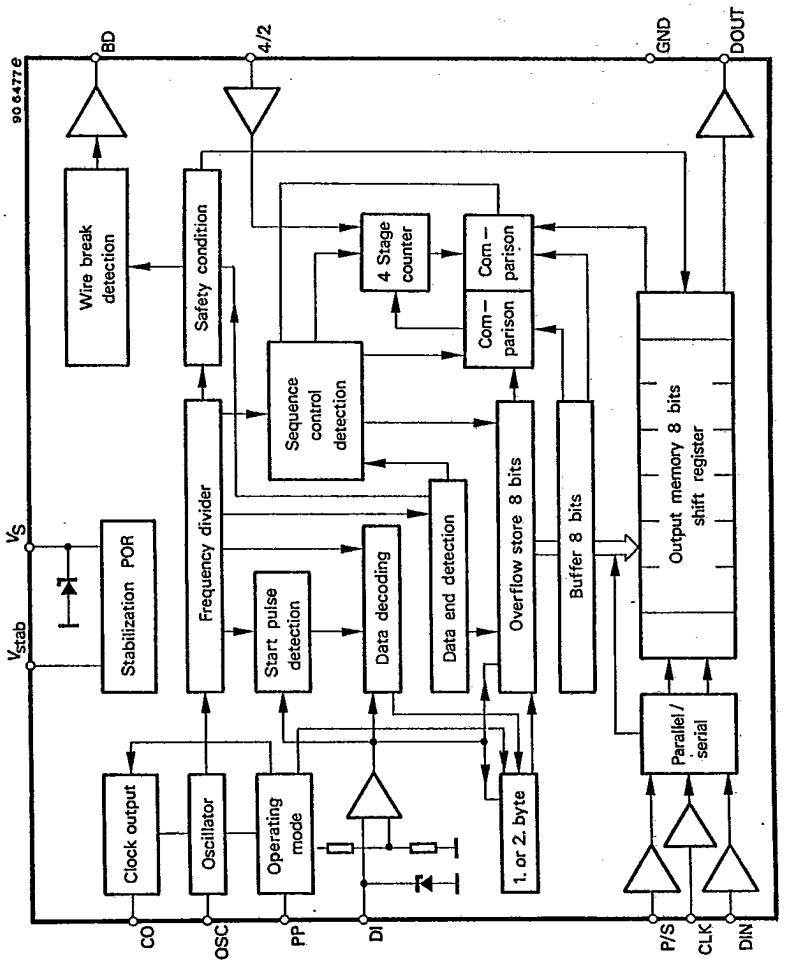

Fig. 2 Block diagram U 6056 B

1. Functional description of transmitter and receiver

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1.1 Power supply

For reasons of protection against interference and surges, all circuits must be equipped with an RC circuit for current limitation in the event of overvoltages and for buffering in the event of voltage dips at V_S.

Suggested dimensions: $R_V = 510\ \Omega$, $C_V = 100\ \mu F$ (Figs. 6 and 13).

An integrated 14 V Z-diode is located between V_S and GND in each case.

1.2 Oscillator

All timing in the circuits is derived from an RC-oscillator in each case; the oscillator's charging time t_1 is determined by an external resistor R_{osc}, and its discharge time t_2 by an integrated 2 kΩ resistor. Since the tolerance and temperature sensitivity of the integrated resistor are considerably greater than those of the external resistor, $t_1/t_2 \geqq 20$ must be selected for stability reasons. The minimum value of R_{osc} should not be less than 68 kΩ.

Recommended frequencies and dimensioning:

$f_{transmitter}$ = 6.4 kHz; C_{osc} = 1 nF; R_{osc} = 200 kΩ
$f_{receiver}$ = 25.6 kHz; C_{osc} = 220 pF; R_{osc} = 200 kΩ

Times derived from the transmitter frequency (6.4 kHz):

Start pulse	: 312 µs
One bit	: 156 µs
Information bit	: 156 µs
Zero bit	: 156 µs
Information unit	: 625 µs
Data word	: 5 ms + 312 µs start bit
Data pause	: 9.688 ms
Transmission cycle	: 15 ms
Minimum reaction time	: 60 ms
Data word master-slave	: 10 ms + 312 µs start bit
Data pause master-slave	: 4.688 ms

1.3 5 V supply

Both the transmitters and receivers can be supplied from one stabilized, noise-free 5 V voltage source. In this case, the series resistor and the filter capacitor are not required. Pin V_{stab} is also supplied by the 5 V supply.
(Figs. 12 and 14).

2. Functional description of the transmitter U 6055 B

The mode of operation corresponds to that of transmitter U 6050 B. The difference is that the U 6055 B cyclically scans the contents of an 8-bit shift register (SR) instead of 8 switches and transmits the result to the receiver as a serial data word via the data line. The SR is normally loaded by a microcomputer.

2.1 Structure of the data word

A switch information unit consists of 4 parts:

1. One bit for receiver synchronization
2. Information bit with "High" = switch open
   "Low" = switch closed
3. Zero bit
4. Zero bit

The data word consists of 2 start bits and 8 information units. For a transmitter frequency of 6.4 kHz, the data word length is 5 ms plus the start pulse, followed by a 10 ms long data interval. The data interval has high potential. When the supply voltage is applied, data transmission is constantly repeated in accordance with this pattern (Fig. 3).

2.2 ON delay and POR

After the supply voltage V_{batt} is applied to the transmitter, a POWER-ON-RESET pulse (POR) is generated internally which sets the logic of the U 6055 B to a basic condition. In contrast to the U 6050 B, the data output is not disabled at the start and is thus immediately ready for operation. The U 6055 B is normally operated with a stabilized voltage in conjunction with a microprocessor.

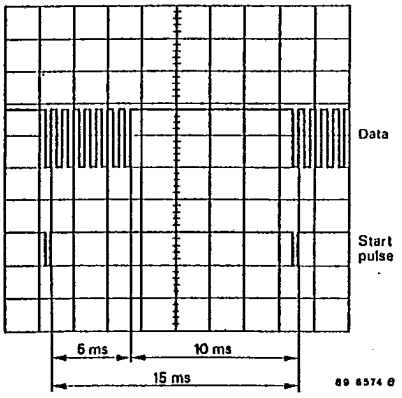

Fig. 3

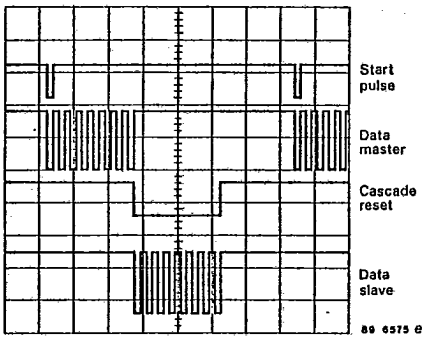

Fig. 4

2.3 Loading the shift register

Loading of the shift register is controlled in the known way by the three inputs DIN, CLK and EN. No data can be inserted in the shift register with EN = "low". If EN = "high", the information from the microprocessor present at the data input DIN is transferred to the shift register with the positive edge of CLK and advanced by one position with every further positive edge from CLK. The eighth flip-flop is a master-slave flip-flop: the information of the eighth flip-flop is transferred to the slave with every negative edge from CLK and is available at the output DOUT.
The information is transferred to the buffer by the negative ENable edge, and only as from this moment is new information transmitted via the data line.
DIN, CLK and EN are high-resistance inputs and possess a switching threshold of approx. 1.8 V. The output DOUT is an open-collector output.
The maximum clock frequency is 50 kHz.

2.4 Cascading (master-slave operation)

Scanning of up to 16 switches or pushbuttons is possible by connecting together two transmitters. The connection between master and slave is shown in Fig. 7. The data output DO of the slave is connected with the data input DIS of the master; the two data signals are combined with each other there and are available at the data output DO of the master (Figs. 4 and 5).

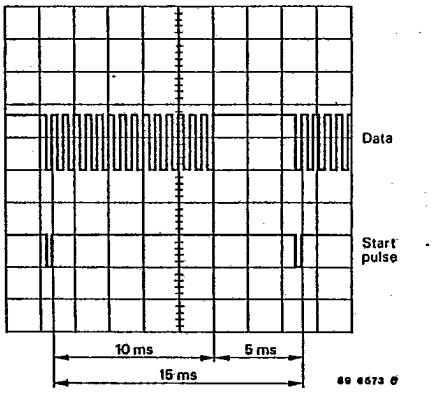

Fig. 5

The master transmits the start bit and the first eight information units; in this time, the frequency divider of the slave is disabled by the master's cascade reset. After the last master information unit, the slave frequency divider is enabled so that the slave scanning cycle and slave data transmission can be performed. In master-slave operation, the data word consists of the start bit and 16 information units (10 ms); the data interval is 5 ms. The clock output CO of the master is connected with the clock input of the slave CI so that the time sequences of both circuits are

synchronous. The voltage supply can be realized with a common series resistor and a common filter capacitor.
Operation with 5 V is possible, refer to Fig. 9.

There are several possibilities of loading the two shift register of master and slave:

a. DIN and CLK of master and slave are parallel-connected. One separate ENable line for master and slave in each case. Loading of the shift registers takes place separately, Fig. 7.

b. CLK and ENable are parallel-connected and $DOUT_{MASTER}$ connected with DIN_{SLAVE}. The data word is loaded as a 16-bit word, Fig. 8.

c. Any combinations of U 6050 B and U 6055 B are possible. Figs. 10 and 11.

2.5 Data output DO

The data output is a push-pull output which is short-circuit proof both with respect to ground and V_{Batt}. The current limiter is set to approx. 30 mA in both cases. A 14 V Z-diode is located between DO and GND to clip interference voltages. For this reason, an external series resistor of 100 Ω is also required to limit the current in the Zener diode.

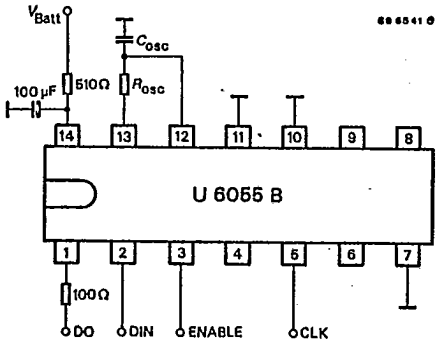

Fig. 6

3. Functional description: receiver U 6056 B

Reception of the information arriving from the transmitter, decoding of the data word and storage in an output memory which can be read out serially via a microprocessor.

3.1 Data decoding

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If a negative edge appears at the data input, the receiver checks whether a start pulse or a fault is present by measuring the duration of the pulse. (A minimum time must be observed). If there is a fault, the receiver waits for the next negative edge.
If it recognises a start pulse, it checks wether an information unit with 8 bits is following and stores this in an 8-bit overflow store. The arriving data are ignored if there is no 8-bit string owing to a fault or a synchronism. The receiver is synchronized by each one bit; scanning of the information takes place in the middle of the information bit. In order to make scanning sufficiently precise, the oscillator frequency of the receiver was selected to be four times as large as that of the transmitter. The deviation of the receiver frequency to the four-fold transmitter frequency may be up to ± 15 % while still guaranteeing reliable data recognition.

3.2 Data check

The data read into the 8-bit overflow store are compared with the contents of the buffer. If they are identical, a 4-stage counter is incremented by one stage: if they are not identical, the counter is reset. The new data combination is transferred to the buffer after each comparison, irrespective of the result.
After coincidence has been established two or four times (programmable pin 2/4), the contents of the buffer are compared with the contents of the output memory. If both are identical, the 4-stage counter is reset and no new information is transferred to the output memory. If the contents of the two memories differ, the data word must have changed and is transferred into the output memory. Since the period of a data transmission is 15 ms, this results in a minimum delay time of 60 ms resp. 30 ms for detection of a change of the data word. Faults on the data line and switch bouncing may lead to an extension of the delay time.
Precondition to transfer the data word into the output memory: Input P/S must be in high potential.

3.3 Safety condition and wire break detection, output BD

If no data reach the receiver owing to a break in the data line or a short-circuit to ground or V_S, all output memories are reset after approx. 50 ms. In this case, output BD assumes low potential as long as data transmission is interrupted. The output BD is an open-collector output.

3.4 Cascading (master-slave operation)

Determination of master or slave is defined by connection of the PP:

Master : PP to V_S

Alone : PP open

Slave : PP to GND

In "master" mode, the oscillator is connected with R_{osc} and C_{osc} and the clock output CO is active. In "slave" mode, the oscillator is blocked and must be activated by the clock output of the master. The master recognises the start bit and decodes the first eight information bits. The slave also recognises the start bit, but decodes the second eight information bits.

There are several possibilities of cascading here as well:

a. CLK and DOUT are parallel-connected in each case. Each shift register can be read out individually by a separate P/S line. Fig. 15.

b. CLK and P/S are parallel-connected in each case. $DOUT_{MASTER}$ and DIN_{SLAVE} are connected with each other. The 16-bit data word can be read out serially via $DOUT_{SLAVE}$ in one operation, Fig. 16.

c. Combinations with U 6051B/U 6052B and U 6056B, Figs. 17 and 18.

3.5 Loading and reading out the shift register

Loading and reading out of data from the shift register is controlled by the three inputs DIN, CLK and P/S:

Inputs P/S = high: Parallel operation; no data can be read out of the shift register. Data which arrive via the data line are stored in the shift register. Output DOUT is disabled (high-resistance).

Input P/S = low: Serial operation; the information available at DIN is transferred to the shift register by the positive edge of CLK and advanced by one position by every further positive edge. The data word appears at DOUT.

The maximum clock frequency is 50 kHz.

The eighth flip-flop is a master-slave flip-flop: the information of the eighth flip-flop is transferred to the slave with every negative edge from CLK and is available at the output DOUT.
DIN, CLK and EN are high-resistance inputs and possess a switching threshold of approx. 1.8 V. The output DOUT is an open-collector output.

3.6 Input 4/2

The number of comparisons can be defined by the wiring configuration of input 4/2:

4-fold comparison : Input 4/2 open
2-fold comparison : Input 4/2 connected to V_S

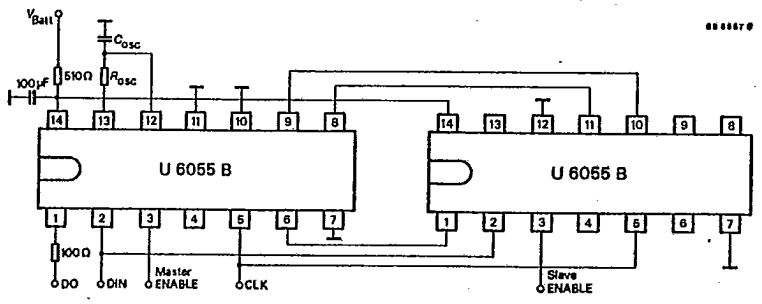


Fig. 7

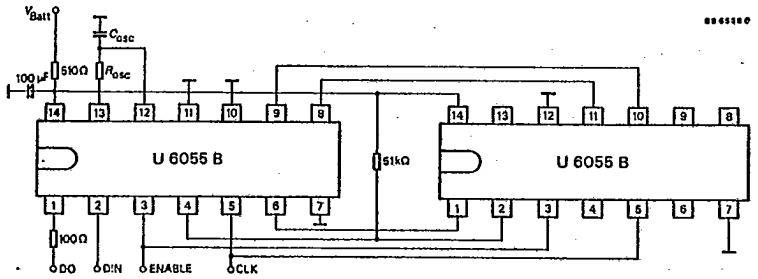


Fig. 8

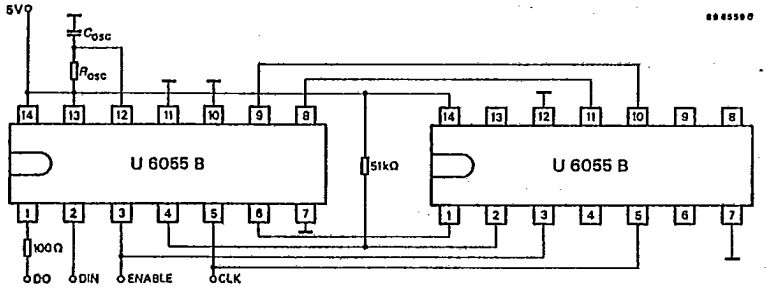


Fig. 9

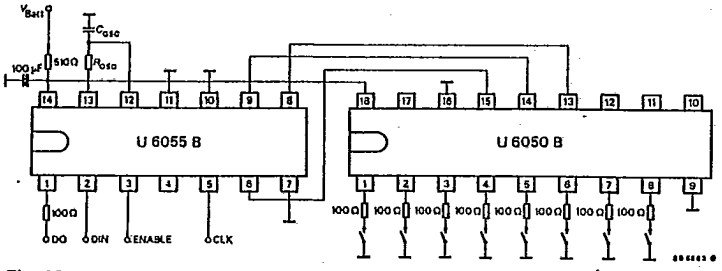


Fig. 10

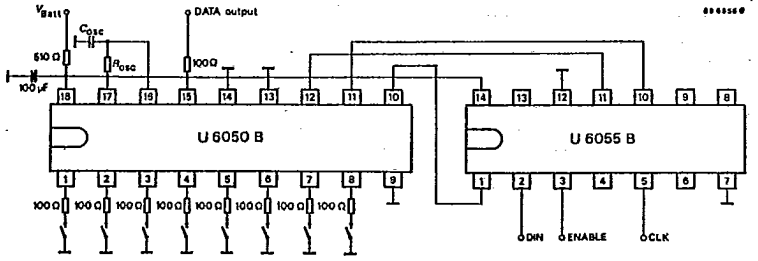


Fig. 11

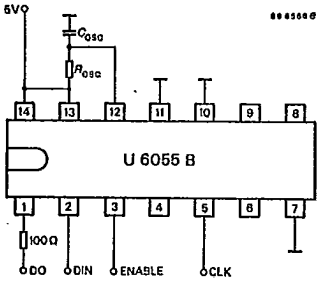


Fig. 12

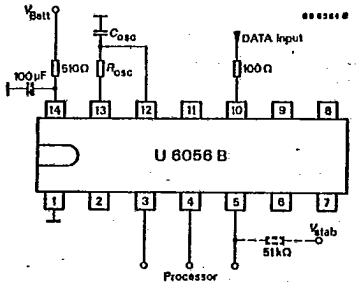


Fig. 13

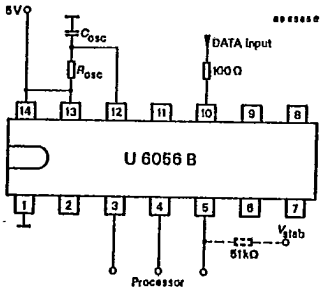


Fig. 14

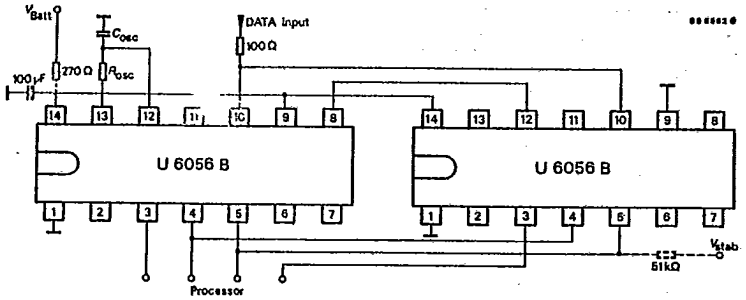


Fig. 15

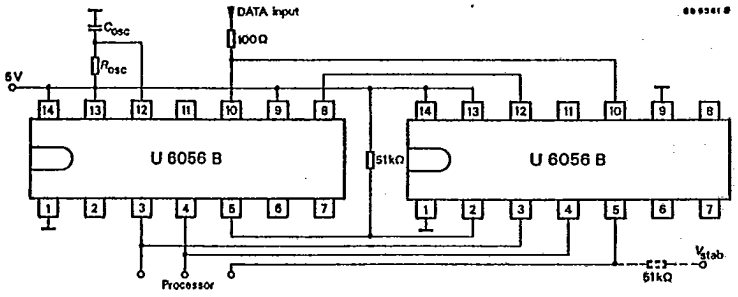


Fig. 16

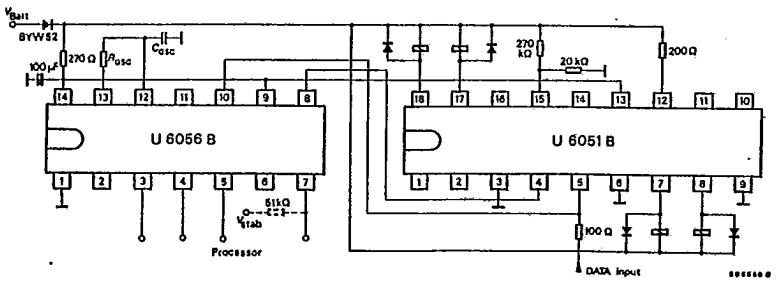


Fig. 17

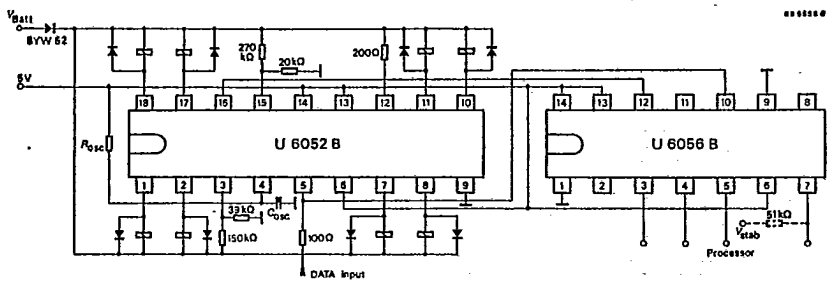


Fig. 18

Pin configuration (U 6055 B)

Pin	Function
1 (1)	Data output DO
2 (3)	Serial data input from microprocessor DIN
3 (4)	Enable input EN
4 (5)	Serial data output DOUT
5 (6)	Clock input from microprocessor CLK
6 (7)	Data input slave DIS
7 (8)	Ground GND
8 (9)	Clock output for cascading CO
9 (10)	Cascading reset output CRO
10 (11)	Cascading reset input CRI
11 (12)	Clock input for cascading CI
12 (13)	RC-oscillator input OSC
13 (14)	Stabilized voltage V_{stab}
14 (16)	Supply voltage V_S
(2,15)	N.C.

Numbers in brackets apply to SO package

Pin configuration (U 6056 B)

Pin	Function
1 (1)	Ground GND
2 (2)	Serial data input of the shift register DIN
3 (4)	Parallel/serial switch-over P/S
4 (5)	Clock input for shift register CLK
5 (7)	Serial data output for the microprocessor DOUT
6 (9)	2/4-fold comparison 2/4
7 (10)	Output wire break detection BD
8 (11)	Clock output for cascading CO
9 (12)	Program pin PP
10 (13)	Data input of data line DT
11 (3,6,8,14,15,16,17)	NC
12 (18)	RC-oscillator input OSC
13 (19)	Stabilized voltage V_{stab}
14 (20)	Supply voltage V_S

U 6055 B Transmitter

Absolute maximum ratings

Transmitter operated with recommended circuitry

Supply voltage (static)		V_S	25	V
Ambient temperature range		T_{amb}	−40...+85	°C
Storage temperature range		T_{stg}	−55...+125	°C
Junction temperature		T_j	150	°C
Power dissipation $T_{amb} = 85$ °C		P_{tot}	720	mW
Maximum thermal resistance				
Junction ambient	DIP 14	R_{thJA}	90	K/W
	SO 16	R_{thJA}	105	K/W

Electrical characteristics		Min.	Typ.	Max.	
V_{Batt} = 13.5 V, T_{amb} = 25 °C, reference point: GND Transmitter operated with recommended circuitry					
Supply voltage	V_{Batt}	6		16	V
5 V supply (without R_V, C_V)	V_S	4.3		6	V
Stabilized voltage	V_{stab}		5.2		V
Protection resistor	R_V	510			Ω
capacitor	C_V		100		µF
POR threshold	V_S	3.0		4.2	V
Current consumption	I_S		1.0		mA
Internal clamping	V_Z		14.3		V
Input Data DIN					
Input Clock CLK					
Input Enable EN					
Treshold voltage	V_{Th}	1.6	1.8	2.1	V
Input current (V_{IN} = 0 V)	$-I_{IN}$			2	µA
Internal pull down-resistor	R_{IN}		100		kΩ
Clock frequency	f_{CLK}			50	kHz
Delay time CLK - D_{out}	t		10		µs
Clock pulse length	t	12			µs
Waiting time between 2 clock ins	t	50			µs
Waiting time EN - CLK	t	1			µs
Oscillator input OSC					
Internal discharge resistor	R_{DIS}	1.6	2.0	2.4	kΩ
Lower threshold	V_{osc}		1.1		V
Upper threshold	V_{osc}		3.3		V
Input current (V_{osc} = 0 V)	$-I_{osc}$			1	µA
Frequency	f_{osc}	1.0	6.4	20	kHz
Clock input CI					
Threshold voltage	V_{CI}		2.0		V
Internal pull down-resistor	R_{CI}		100		kΩ
Input current (V_{CI} = 0 V)	$-I_{CI}$			2	µA

		Min.	Typ.	Max.	
Clock output CO					
Output current "high" (V_{CO} = 0 V)	$-I_{CO}$			150	µA
Saturation voltage "low" (150 µA)	V_{CO}			0.3	V
Current capability	I_{CO}			1	mA
Cascade reset input CRI					
Threshold voltage	V_{CRI}		2.0		V
Internal pull down resistor	R_{CRI}		100		kΩ
Input current	$-I_{CRI}$			2	µA
V_{CRI} = 0 V: normal operation V_{CRI} = V_S : reset status					
Cascade reset output CRO					
Output current "high" (V_{CRO} = 0 V)	$-I_{CRO}$			150	µA
Saturation voltage "low" (150 µA)	V_{CRO}			0.3	V
Current capability	I_{CRO}			1	mA
Data output DO					
Saturation voltage "low" (10 mA))	V_{DO}			1.5	V
Saturation voltage "high" (10 mA)	V_{DO}/V_S			2.4	V
Current limitation (V_{DO} = 0 V) (V_{DO} = V_{Batt})	$-I_{DO}$ I_{DO}		30 30		mA mA
Internal clamping	V_Z		14.3		V
External protection resistor	R_{DO}	100			Ω
Data input slave DIS					
Internal pull up resistor	R_{DIS}		100		kΩ
Detection treshold	V_{DIS}		2.0		V
Serial data output DOUT – open collector –					
Saturation voltage (1 mA)	V_{DOUT}			0.2	V
Current capability	I_{DOUT}			1	mA
Reverse current	I_{DOUT}			5	µA
Rise time, R_1 = 51 kΩ	t		2		µs
Fall time, R_1 = 51 kΩ	t		200		ns

U 6056 B Receiver

Absolute maximum ratings

Receiver with recommended circuitry

Supply voltage (static)	V_S	25	V
Ambient temperature range	T_{amb}	−40...+85	°C
Storage temperature range	T_{stg}	−55...+125	°C
Junction temperature	T_j	150	°C
Power dissipation $T_{amb} = 85$ °C	P_{tot}	720	mW

Maximum thermal resistance

Junction ambient	DIP 14	R_{thJA}	90 K/W
	SO 20	R_{thJA}	100 K/W

Electrical characteristics

$V_{Batt} = 13.5$ V, $T_{amb} = 25$ °C, reference point: GND

Receiver operated with recommended circuitry

		Min.	Typ.	Max.	
Supply voltage	V_{Batt}	6		16	V
5 V supply (without R_V, C_V)	V_S	4.3		6	V
Stabilized voltage	V_{stab}		5.2		V
Protection resistor	R_V	510			Ω
capacitor	C_V		100		µF
POR threshold	V_S	3.0		4.2	V
Current consumption	I_S		1.5	2.0	mA
Internal clamping	V_Z		14.3		V

Input Data DIN

Input Clock CLK

Input Parallel, Serial P/S

Threshold voltage	V_{Th}	1.6	1.8	2.1	V
Input current ($V_{IN} = 0$ V)	$-I_{IN}$			2	µA
Internal pull down resistor	R_{IN}		100		kΩ
Clock frequency	f_{CLK}			50	kHz
Delay time CLK-D_{out}	t		10		µs
Clock pulse length	t	12			µs
Waiting time between 2 readings	t	40/80			ms
Waiting time EN−CLK	t	1			µs

		Min.	Typ.	Max.	
Serial data output DOUT					
Saturation voltage (1 mA)	V_{DOUT}			0.2	V
Current capability	I_{DOUT}			1	mA
Reverse current	I_{DOUT}			5	µA
Rise time, $R_1 = 51$ kΩ	t		2		µs
Fall time, $R_1 = 51$ kΩ	t		200		ns
Oscillator input OSC					
Internal discharge resistor	R_{DIS}	1.6		2.4	kΩ
Lower threshold	V_{OSC}		1.1		V
Upper threshold	V_{OSC}		3.3		V
Input current ($V_{OSC} = 0$ V)	$-I_{OSC}$		1		µA
Frequency	f_{OSC}	1.0	25.6	50.0	kHz
Data input DI					
Threshold voltage	V_{DI}		$0.5 \cdot V_S$		V
Internal pull down resistor	R_{DI}		100		kΩ
Internal clamping	V_Z		14.3		V
Input current ($V_{DI} = 0$ V)	$-I_{DI}$			1	µA
External protection	R_{DI}	100			Ω
Program pin PP					
Lower threshold	V_{PP}		$0.24 \cdot V_S$		V
Upper threshold	V_{PP}		$0.50 \cdot V_S$		V
Pin PP open	V_{PP}		$0.37 \cdot V_S$		V
Input current					
($V_{PP} = 0$ V)	$-I_{PP}$		50		µA
($V_{PP} = V_S$)	I_{PP}		50		µA

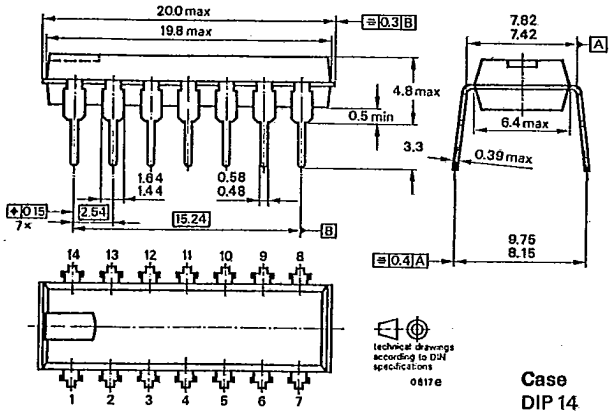
Pin PP:	operation mode
open	single
GND	slave
V_S	master

Clock output CO					
Output current "high" ($V_{CO} = 0$ V)	$-I_{CO}$			150	µA
Saturation voltage "low" (150 µA)	V_{CO}			1	V

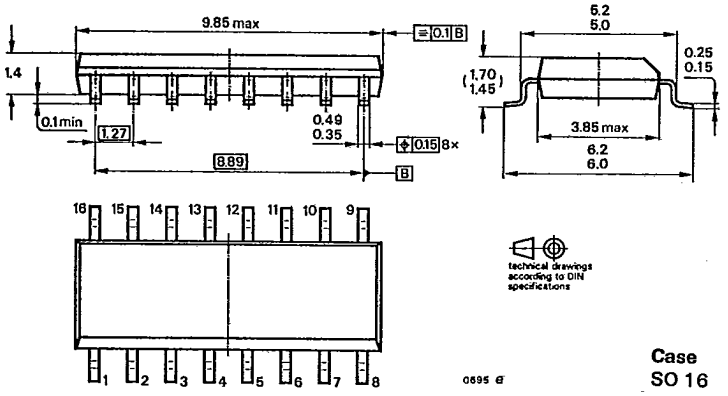
		Min.	Typ.	Max.	
Wire break detection BD (open collector)					
Saturation voltage (1 mA)	V_{BD}			0.2	V
Current capability	I_{BD}			1	mA
Reverse current	I_{BD}			5	µA
Input 2/4					
Threshold voltage	$V_{2/4}$	1.6	1.8	2.1	V
Input current ($V_{2/4} = 0$ V)	$-I_{2/4}$			2	µA
Internal pull down resistor	$R_{2/4}$		100		kΩ

Pin 2/4 open : 4-fold comparison
Pin 2/4 to V_S : 2-fold comparison

Dimensions in mm



Case
DIP 14

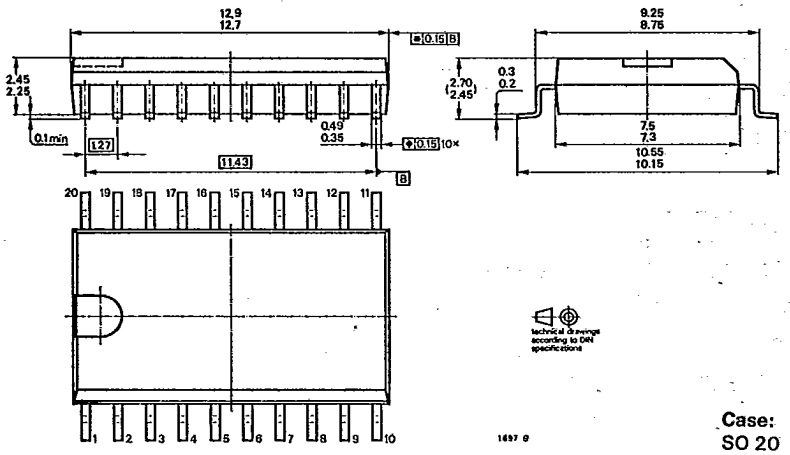


Case
SO 16

U 6055 B · U 6056 B

T-75-45-07

Dimensions in mm



Case:
SO 20