NEC

NEC Electronics Inc.

μPD27C64
8,192 x 8-BIT
CMOS UV/OTP EPROM

Revision 1

January 1986

Description

The μPD27C64 is a 65,536-bit (8,192 × 8-bit) electrically programmable read-only memory (EPROM). It operates from a single +5 V power supply making it ideal for microprocessor applications. It is fabricated using an advanced CMOS process which saves substantial power in operating and standby modes.

A distinctive feature of the μPD27C64 is an output enable (OE) separate from the chip enable (CE). The OE control eliminates bus contention in multiple-bus microprocessor systems. The μPD27C64 features fast, simple, one-pulse programming controlled by TTL-level signals. A high-speed programming mode is also available.

The μPD27C64 is available in a cerdip package with a quartz window as an ultraviolet (UV), erasable EPROM, or in a plastic package as a one-time-programmable (OTP), non-erasable EPROM.

Features

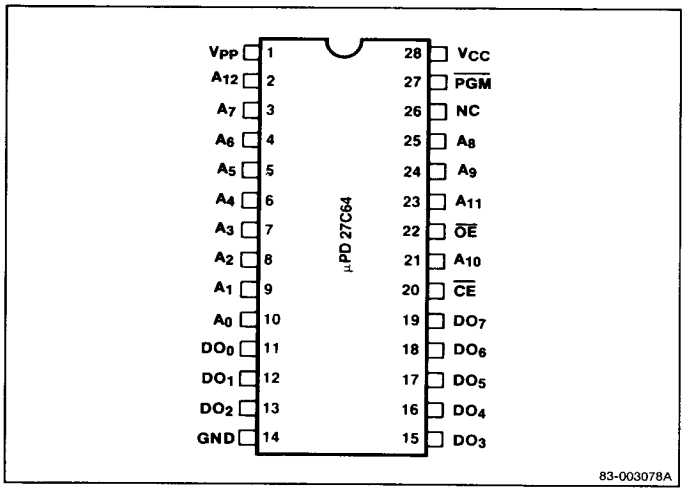
- ☐ Ultraviolet erasable and electrically programmable
- ☐ Low supply current:
  - — 30 mA (max) active current
  - — 100 μA (max) standby current
- ☐ High-speed programming mode
- ☐ Single location programming
- ☐ Programmable with single pulse (total programming time is 420 sec in standard mode)
- ☐ Input/output TTL-compatible
- ☐ Single +5 V power supply
- ☐ Low power dissipation:
  - — 33 mW/MHz (max) operating
  - — 550 μW (max) standby
- ☐ μPD2764-compatible
- ☐ 28-pin DIP

Performance Ranges

Device	Access Time (Max)	Power Supply (Max) Active	Standby
μPD27C64-20	200 ns	30 mA	100 μA
μPD27C64-25(1)	250 ns	30 mA	100 μA
μPD27C64-30(1)	300 ns	30 mA	100 μA

Note:
(1) Available as either UV or OTP.

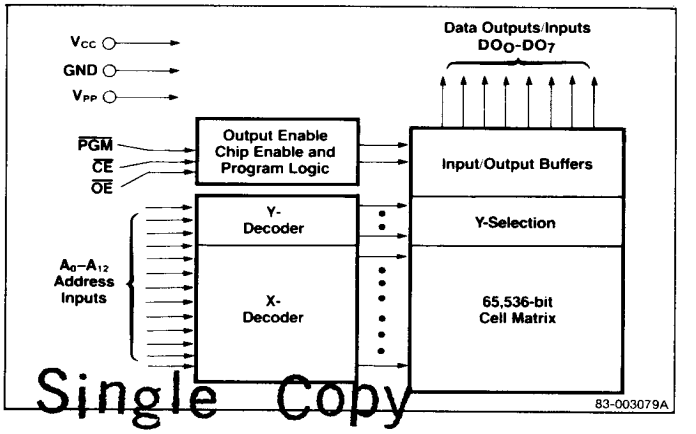
Pin Configuration



Pin Identification

No.	Symbol	Function
1	V_{PP}	Program voltage
2–10, 21, 23–25	A_0–A_{12}	Address inputs
11–13, 15–19	DO_0–DO_7	Data inputs / outputs
14	GND	Ground
20	$\overline{CE}$	Chip enable
22	$\overline{OE}$	Output enable
26	NC	No connection
27	$\overline{PGM}$	Program
28	V_{CC}	+5 V power supply

Block Diagram



Absolute Maximum Ratings

Power supply voltage, V_{CC}	−0.3 V to +7.0 V
Input voltage, V_{IN}	−0.3 V to V_{CC} + 0.3 V
Output voltage, V_{OUT}	−0.3 V to V_{CC} + 0.3 V
Operating temperature, T_{OPR}	−10°C to +80°C
Storage temperature, T_{STG}	−65°C to +125°C
Program voltage, V_{PP}	−0.3 V to +22 V

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of the specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

$T_A = 25°C$, f = 1 MHz

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_{IN}			6	pF	$V_{IN} = 0$ V
Output capacitance	C_{OUT}			12	pF	$V_{OUT} = 0$ V

DC Characteristics

Read and Standby Modes

$T_A = 0°C$ to +70°C, $V_{CC} = +5$ V ± 10%, $V_{PP} = V_{CC}$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	2.4			V	$I_{OH} = -400\ \mu A$
Output voltage, low	V_{OL}			0.45	V	$I_{OL} = 2.1$ mA
Input voltage, high	V_{IH}	2.0		$V_{CC}+0.3$	V	
Input voltage, low	V_{IL}	−0.3		0.8	V	
Output leakage current	I_{LO}			10	μA	$\overline{OE} = V_{IH}$, $V_{OUT} = 0$ V to V_{CC}
Input leakage current	I_{LI}			10	μA	$V_{IN} = 0$ V to V_{CC}
Operating supply current	I_{CCA1}			10	mA	$\overline{CE} = V_{IL}$, $V_{IN} = V_{IH}$
Operating supply current	I_{CCA2}			30	mA	f = 5 MHz, $I_{OUT} = 0$ mA
Standby supply current	I_{CCS1}			1	mA	$\overline{CE} = V_{IH}$
Standby supply current	I_{CCS2}		1	100	μA	$\overline{CE} = V_{CC}$, $V_{IN} = 0$ V to V_{CC}
Program voltage current	I_{PP1}		1	100	μA	$V_{PP} = V_{CC} \pm 0.6$ V

Standard Programming, Program Verify, and Program Inhibit Modes

$T_A = 25°C \pm 5°C$, $V_{CC} = +5$ V ± 10%, $V_{PP} = +21$ V ± 0.5 V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	2.4			V	$I_{OH} = -400\ \mu A$
Output voltage, low	V_{OL}			0.45	V	$I_{OL} = 2.1$ mA
Input voltage, high	V_{IH}	2.0		$V_{CC}+0.3$	V	
Input voltage, low	V_{IL}	−0.3		0.8	V	
Input leakage current	I_{LI}			10	μA	$V_{IN} = V_{IL}$ or V_{IH}
Operating supply current	I_{CC2}			30	mA	
Program voltage current	I_{PP}			30	mA	$\overline{CE} = \overline{PGM} = V_{IL}$

High-Speed Programming Mode

$T_A = 25°C \pm 5°C$, $V_{CC} = +6$ V ± 0.25 V, $V_{PP} = +21$ V ± 0.5 V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	2.4			V	$I_{OH} = -400\ \mu A$
Output voltage, low	V_{OL}			0.45	V	$I_{OL} = 2.1$ mA
Input voltage, high	V_{IH}	2.0		$V_{CC}+1$	V	
Input voltage, low	V_{IL}	−0.1		0.8	V	
Input leakage current	I_{LI}			10	μA	$V_{IN} = V_{IL}$ or V_{IH}
Operating supply current	I_{CC2}			30	mA	
Program voltage current	I_{PP}			30	mA	$\overline{CE} = \overline{PGM} = V_{IL}$

AC Characteristics

Read and Standby Modes

$T_A = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 10\%$, $V_{PP} = V_{CC}$

Parameter	Symbol	Limits μPD27C64-20 Min	Limits μPD27C64-20 Max	Limits μPD27C64-25(1) Min	Limits μPD27C64-25(1) Max	Limits μPD27C64-30(1) Min	Limits μPD27C64-30(1) Max	Unit	Test Conditions(2)
Address to output delay	t_{ACC}		200		250		300	ns	$\overline{CE} = \overline{OE} = V_{IL}$
$\overline{CE}$ to output delay	t_{CE}		200		250		300	ns	$\overline{OE} = V_{IL}$
$\overline{OE}$ low to data output delay	t_{OE}	10	75	10	100	10	120	ns	$\overline{CE} = V_{IL}$
$\overline{OE}$ high to data output float delay	t_{DF}	0	60	0	85	0	105	ns	$\overline{CE} = V_{IL}$
Address to output hold time	t_{OH}	0		0		0		ns	$\overline{CE} = \overline{OE} = V_{IL}$

Note:

(1) Available in either UV or OTP.

(2) Output load: see Loading Conditions Test Circuit. Input rise and fall times: 20 ns. Input pulse levels: 0.45 V to 2.4 V. Timing measurement reference levels:
Inputs: 0.8 V and 2.0 V
Outputs: 0.8 V and 2.0 V.

Standard Programming, Program Verify, and Program Inhibit Modes

$T_A = 25°C \pm 5°C$, $V_{CC} = +5V \pm 10\%$, $V_{PP} = +21V \pm 0.5V$

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
Address setup time	t_{AS}	2			μs	(Notes 1, 2, 3)
Data setup time	t_{DS}	2			μs	(Notes 1, 2, 3)
Address hold time	t_{AH}	0			μs	(Notes 1, 2, 3)
Data hold time	t_{DH}	2			μs	(Notes 1, 2, 3)
Output enable to output float delay	t_{DF}	0		130	ns	(Notes 1, 2, 3)
Program supply setup time	t_{VS}	2			μs	(Notes 1, 2, 3)
Program pulse width	t_{PW}	20	50	55	ms	(Notes 1, 2, 3)
$\overline{CE}$ setup time	t_{CES}	2			μs	(Notes 1, 2, 3)
$\overline{OE}$ setup time	t_{OES}	2			μs	(Notes 1, 2, 3)
$\overline{OE}$ to data utilization delay	t_{OE}			150	ns	(Notes 1, 2, 3)

Note:

(1) Input pulse levels: $V_I = 0.45V$ to 2.4 V.

(2) Input and output timing reference levels = 0.8 V and 2.0 V.

(3) Input rise and fall times = 20 ns.

High-Speed Programming Mode

$T_A = 25°C \pm 5°C$, $V_{CC} = +6V \pm 0.25V$, $V_{PP} = +21V \pm 0.5V$

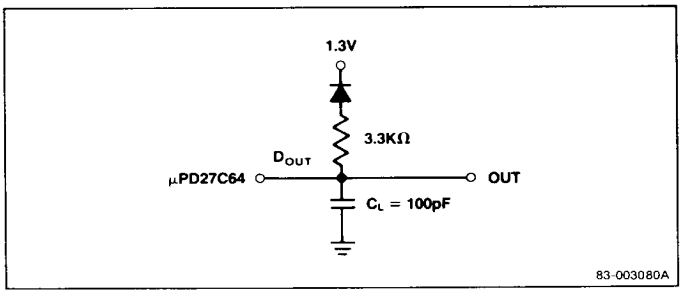
Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
Address setup time	t_{AS}	2			μs	(Notes 1, 2)
Data setup time	t_{DS}	2			μs	(Notes 1, 2)
Address hold time	t_{AH}	2			μs	(Notes 1, 2)
Data hold time	t_{DH}	2			μs	(Notes 1, 2)
Chip enable to output float delay	t_{DF}	0		130	ns	(Notes 1, 2)
Supply current setup time	t_{VCS}	2			μs	(Notes 1, 2)
Program setup time	t_{VPS}	2			μs	(Notes 1, 2)
Initial program pulse width	t_{PW}	0.95	1	1.05	ms	(Notes 1, 2)
Additional program pulse range	t_{OPW}	3.8		63	ms	(Notes 1, 2)
$\overline{CE}$ setup time	t_{CES}	2			μs	(Notes 1, 2)
$\overline{OE}$ setup time	t_{OES}	2			μs	(Notes 1, 2)
$\overline{OE}$ data utilization delay	t_{OE}			150	ns	(Notes 1, 2)

Note:

(1) Input pulse levels: $V_I = 0.45V$ to 2.4 V.

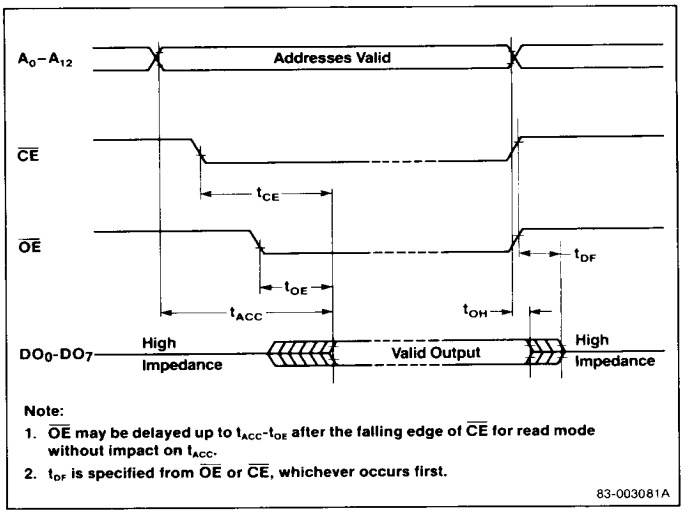
(2) Input and output timing reference levels = 0.8 V and 2.0 V.

Figure 1. Loading Conditions Test Circuit



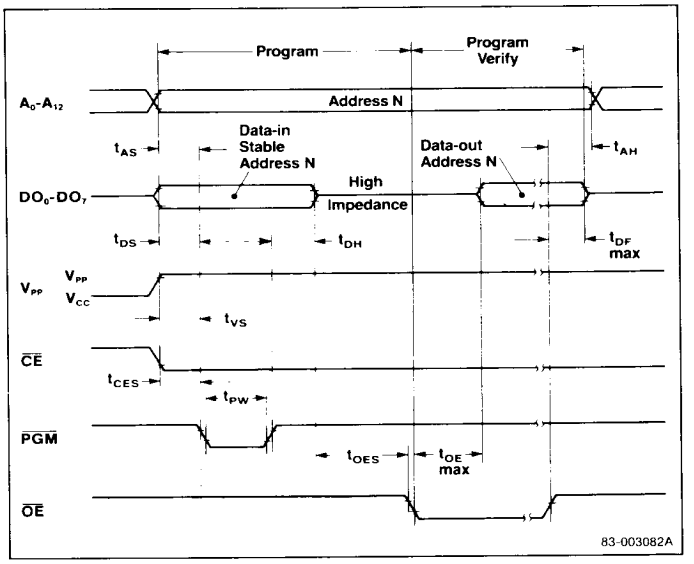
Timing Waveforms

Read Mode

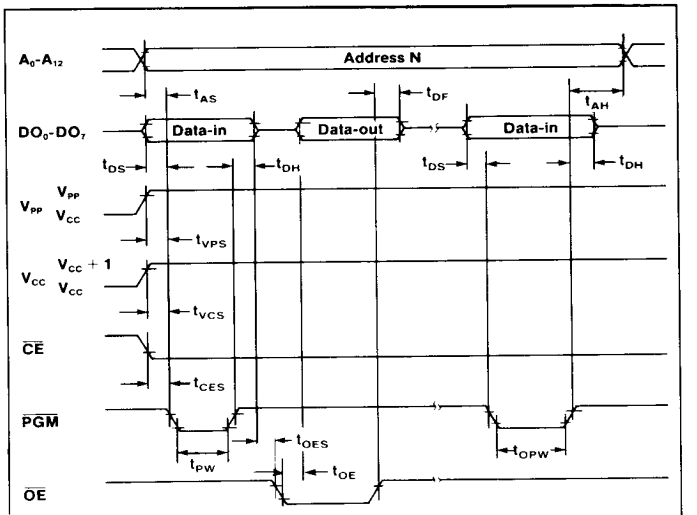


Note:
1. $\overline{OE}$ may be delayed up to $t_{ACC}-t_{OE}$ after the falling edge of $\overline{CE}$ for read mode without impact on t_{ACC}.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

Programming Mode



High-Speed Programming Mode



Note:
1. If a read is performed within the t_{ACC} range, the $\overline{OE}$ input lead time from $\overline{CE}$ fall time is $t_{ACC}-t_{OE}$ [max].
2. t_{DF} represents the time from the rise of $\overline{OE}$ or $\overline{CE}$, whichever rises to V_{IH} first.
3. Connect V_{CC} before V_{PP} and disconnect after V_{PP}.

83-003083A

Truth Table

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	V_{IH}	+5 V	+5 V	Data output
Standby	V_{IH}	X	X	+5 V	+5 V	High impedance
Standard program	V_{IL}	X	V_{IL}	V_{PP}	+5 V	Data input
Program verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	+5 V	Data output
Program inhibit	V_{IH}	X	X	V_{PP}	+5 V	High impedance
High-speed programming	V_{IL}	X	V_{IL}	V_{PP}	+6 V	Data input

Note:
(1) X can be either V_{IL} or V_{IH}. (V_{IH} = TTL-level high input voltage, V_{IL} = TTL-level low input voltage)

Function

The μPD27C64 uses a single standard +5 V power supply (μPD8086, μPD8085, μPD8088). Furthermore, all the input/output terminals are TTL-level so that the total system can be simplified. For programming purposes, an additional +21 V power supply is required.

The μPD27C64 does not require any complex programming devices. Programming can be done while chips are mounted on a system board. A single TTL-level pulse (pulse duration 50 ms) is used to program any single address.

The μPD27C64 features a standby mode which reduces the power dissipation from the maximum active power dissipation of 165 mW to a maximum standby power dissipation of 550 μW. This results in a power savings of over 99% with no increase in access time.

Erasure

Data written on the μPD27C64 can be erased by light with a wavelength shorter than 400 nm. If it is exposed to direct sunlight or fluorescent light, programmed data may be erased. Therefore, in order to protect the programmed data, mask the window to prevent erasing by ultraviolet rays.

Data on the μPD27C64 is usually erased by 254 nm ultraviolet rays. The lighting level required to completely erase written data is 15 W-sec/cm^2 (min) (ultraviolet ray intensity × exposure time).

An ultraviolet lamp of 12,000 μW/cm^2 will take approximately 15 to 20 minutes. The distance between the lamp and μPD27C64 should be within 2.5 cm. The filter on the ultraviolet lamp should be removed for this operation. The program protect seal should also be removed from the window of the μPD27C64.

Operation

The six operation modes of the μPD27C64 are listed in the truth table. V_{CC} should be set to +5 V for each Read, Standby, Standard programming, Program verify, or Program inhibit mode. V_{CC} should be set to +6 V for the High-speed Programming mode. Control terminals $\overline{CE}$, $\overline{OE}$, $\overline{PGM}$, and V_{PP} should be set according to the data in this table.

Read Mode

When $\overline{CE}$ and $\overline{OE}$ are at a low (0) level, Read is set and data is available at the outputs after t_{OE} from the falling edge of $\overline{OE}$ and t_{ACC} after setting the address.

Standby Mode

The μPD27C64 is placed in a standby mode with the application of a high (1) level TTL signal to the $\overline{CE}$ input. In this mode the outputs are in a high-impedance state, independent of the $\overline{OE}$ input. The active power dissipation is reduced from 165 mW to 550 μW.

Programming Modes

The μPD27C64 can be programmed in two ways: (1) standard programming mode, and (2) high-speed programming mode. In the standard mode, basically a 50 ms $\overline{PGM}$ pulse is applied to each bit location. The high-speed programming mode is similar to the Intelligent Programming Algorithm® in which up to fifteen 1 ms $\overline{PGM}$ pulses are applied to each bit location, followed by an additional $\overline{PGM}$ pulse, of which the width is 4 ms for each number of 1 ms pulses applied before. The high-speed programming mode reduces the programming time to typically 60 s to 120 s.

Standard Programming Mode

Programming begins by erasing all data and consequently having all bits in the high (1) level state. Data is then entered by programming a low (0) level TTL signal into the chosen bit location.

The μPD27C64 is placed in the programming mode by applying a low (0) TTL-level program pulse to the $\overline{CE}$ and $\overline{PGM}$ inputs with V_{PP} at +21 V. The data to be programmed is applied to the output pins in 8-bit parallel form at TTL levels.

Any location can be programmed at any time, either individually, sequentially, or at random.

When multiple μPD27C64s are connected in parallel except for $\overline{CE}$, individual μPD27C64s can be programmed by applying a low (0) level TTL pulse to the $\overline{PGM}$ input of the desired μPD27C64 to be programmed.

Programming of multiple μPD27C64s in parallel with the same data is easily accomplished. All the like inputs are tied together and programmed by applying a low (0) level TTL pulse to the $\overline{PGM}$ inputs.

High-speed Programming Mode

In this mode, programming begins by addressing the first location, and applying valid data to the eight output pins (a low-level TTL signal, 0, into the chosen bit location).

V_{CC} is then raised to 6 V ± 0.25 V followed by V_{PP} raised to 21 V ± 0.5 V. A $\overline{PGM}$ pulse of 1 ms ± 5% is then input in the same manner as described in the programming mode timing diagram. The bit is then verified and a program/no-program decision is made. If the bit is not yet programmed, another 1 ms $\overline{PGM}$ pulse is input, to a maximum of fifteen times. If the bit is programmed within fifteen efforts, another pulse of 4 ms for each effort is input and the next address is input. If the bit does not program within fifteen 1 ms efforts, another $\overline{PGM}$ pulse of 60 ms is input and the bit verified. If the bit is not programmed at this stage, the device would be rejected as a program failure. If the bit is programmed, the next address is input until all addresses are complete.

At this stage, V_{CC} and V_{PP} pins are lowered to 5 V ± 5% and all bytes are then verified again for programming.

® Intelligent Programming Algorithm is a registered trademark of Intel Corporation.

Program Inhibit Mode

Programming multiple μPD27C64s in parallel with different data is easier with the programming inhibit mode. Except for $\overline{CE}$ (or $\overline{PGM}$) all like inputs (including $\overline{OE}$) of the parallel μPD27C64s may be common. Programming is accomplished by applying a low (0) TTL-level program pulse to the $\overline{CE}$ and $\overline{PGM}$ inputs with V_{PP} at +21V. A high (1) level applied to the $\overline{CE}$ (or $\overline{PGM}$) of the other μPD27C64 will inhibit it from being programmed.

Program Verify Mode

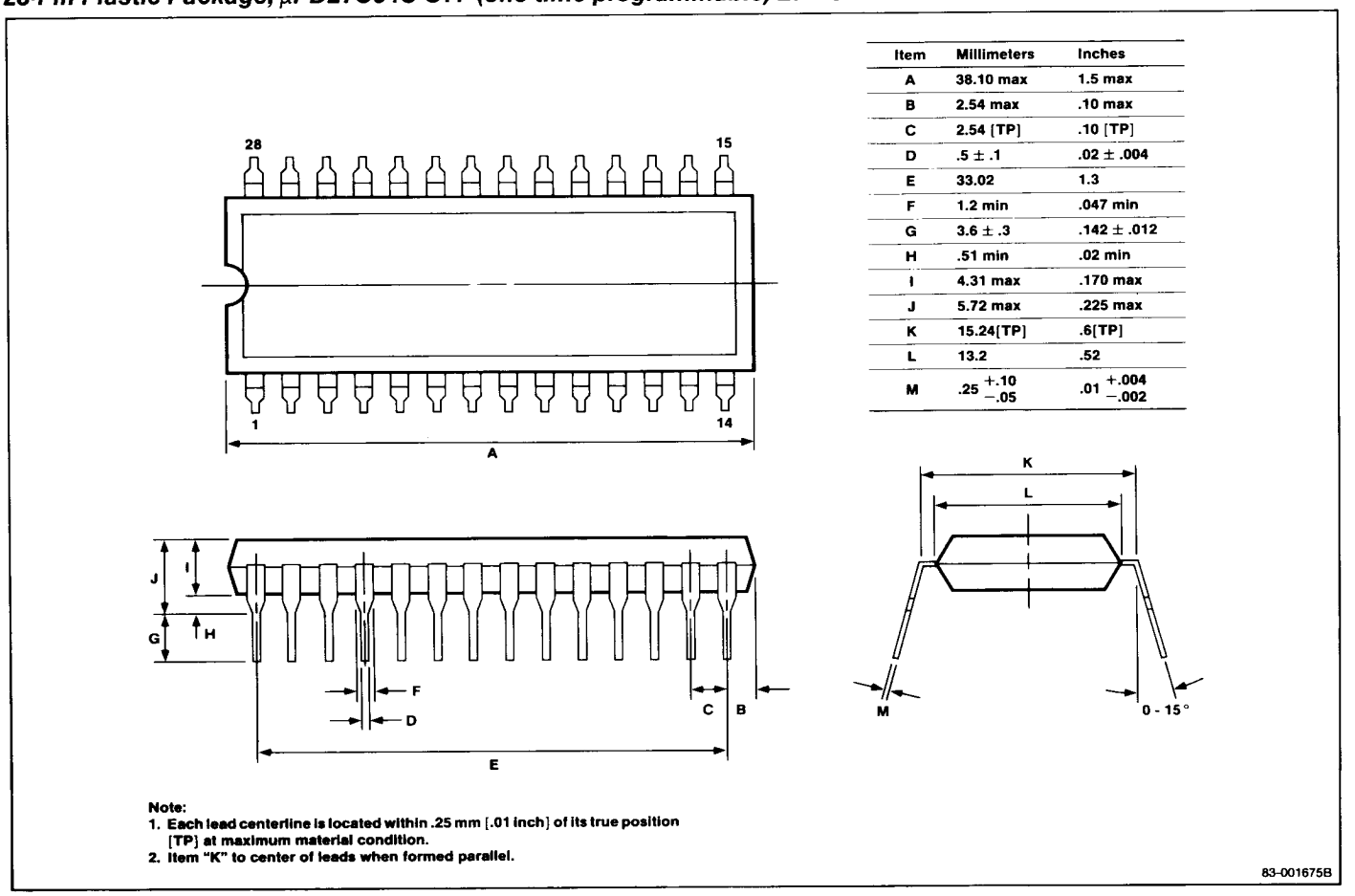
A verify should be performed on the programmed bits to determine that the data was correctly programmed. The program verify can be performed with $\overline{CE}$ and $\overline{OE}$ at low (0) levels and $\overline{PGM}$ at a high (1) level.

Output Disable

The data outputs of two or more μPD27C64s may be wire-ORed together to the same data bus. In order to prevent bus contention problems between devices, all but the selected μPD27C64s should be disabled by raising the $\overline{CE}$ input to a TTL high. $\overline{OE}$ input should be made common to all devices and connected to the read line from the system control bus. These connections offer the lowest average power consumption.

Packaging Information

28-Pin Plastic Package, μPD27C64C OTP (one-time programmable) EPROM



Item	Millimeters	Inches
A	38.10 max	1.5 max
B	2.54 max	.10 max
C	2.54 [TP]	.10 [TP]
D	.5 ± .1	.02 ± .004
E	33.02	1.3
F	1.2 min	.047 min
G	3.6 ± .3	.142 ± .012
H	.51 min	.02 min
I	4.31 max	.170 max
J	5.72 max	.225 max
K	15.24[TP]	.6[TP]
L	13.2	.52
M	$.25^{+.10}_{-.05}$	$.01^{+.004}_{-.002}$

Note:
1. Each lead centerline is located within .25 mm [.01 inch] of its true position [TP] at maximum material condition.
2. Item "K" to center of leads when formed parallel.

83-001675B

REGIONAL SALES AND ENGINEERING SUPPORT OFFICES

NORTHEAST
Twenty Burlington Mall Road, Suite 449
Burlington, MA 01803
TEL 617-272-1774 TWX 710-348-6515

SOUTHEAST
Radice Corporate Center
600 Corporate Drive, Suite 412
Fort Lauderdale, FL 33334
TEL 305-776-0682 TWX 759839

MIDWEST
3025 West Salt Creek Lane, Suite 300
Arlington Heights, IL 60005
TEL 312-577-9090 TWX 910-687-1492

SOUTHCENTRAL
16475 Dallas Parkway, Suite 380
Dallas, TX 75248
TEL 214-931-0641 TWX 910-860-5284

SOUTHWEST
200 East Sandpointe, Building 8 Suite 460
Santa Ana, CA 92707
TEL 714-546-0501 TWX 759845

NORTHWEST
10080 North Wolfe Road, SW3 Suite 360
Cupertino, CA 95014
TEL 408-446-0650 TLX 595497

DISTRICT OFFICES

200 Broadhollow Road, Suite 302
Route 110
Melville, NY 11747
TEL 516-423-2500 TWX 510-224-6090

Beechwood Office Park
385 South Road
Poughkeepsie, NY 12601
TEL 914-452-4747 TWX 510-248-0066

200 Perinton Hills Office Park
Fairport, NY 14450
TEL 716-425-4590 TWX 510-100-8949

5720 Peachtree Parkway, Suite 120
Norcross, GA 30092
TEL 404-447-4409 TWX 910-997-0450

7257 Parkway Drive, Suite 109
Hanover, MD 21076
TEL 301-796-3944 TLX 759847

29200 Southfield Road, Suite 208
Southfield, MI 48076
TEL 313-559-4242 TWX 810-224-4625

Busch Corporate Center
6480 Busch Blvd., Suite 121
Columbus, OH 43229
TEL 614-436-1778 TWX 510-101-1771

8030 Cedar Avenue South, Suite 229
Bloomington, MN 55420
TEL 612-854-4443 TWX 910-997-0726

DISTRICT OFFICES [cont]

Echelon Building 2
9430 Research Boulevard, Suite 330
Austin, TX 78759
TEL 512-346-9280

6150 Canoga Avenue, Suite 112
Woodland Hills, CA 91367
TEL 818-716-1535 TWX 559210

Lincoln Center Building
10300 S.W. Greenburg Road, Suite 540
Portland, OR 97223
TEL 503-245-1600

5445 DTC Parkway, Suite 218
Englewood, CO 80111
TEL 303-694-0041 TWX 510-600-5666

NATICK TECHNOLOGY CENTER

One Natick Executive Park
Natick, MA 01760
TEL 617-655-8833 TWX 710-386-2110

NEC
NEC Electronics Inc.
CORPORATE HEADQUARTERS
401 Ellis Street
P.O. Box 7241
Mountain View, CA 94039
TEL 415-960-6000
TWX 910-379-6985

NECEL-000239-0186
STOCK NO. 600725