NEC
NEC Electronics Inc.

μPD41464
65,536 x 4-BIT
DYNAMIC NMOS RAM

November 1987

Description

The μPD41464 is a 65,536-word by 4-bit dynamic N-channel MOS random access memory (RAM) designed to operate from a single +5-volt power supply. The negative voltage substrate bias is generated internally; its operation is automatic and transparent. The μPD41464 utilizes double-polylayer, N-channel silicon gate processing, which provides high storage cell density, high performance, and high reliability. The device also uses a single-transistor dynamic storage cell and advanced dynamic circuitry throughout, ensuring minimum power dissipation.

The three-state I/O is controlled by $\overline{CAS}$ independent of $\overline{RAS}$. After a valid read or hidden refresh cycle, data is held on the I/O by holding $\overline{CAS}$ low. The data I/O is returned to the high-impedance state by returning $\overline{CAS}$ high. The μPD41464 hidden refresh feature allows $\overline{CAS}$ to be held low to maintain output data while $\overline{RAS}$ is used to execute $\overline{RAS}$-only refresh cycles.

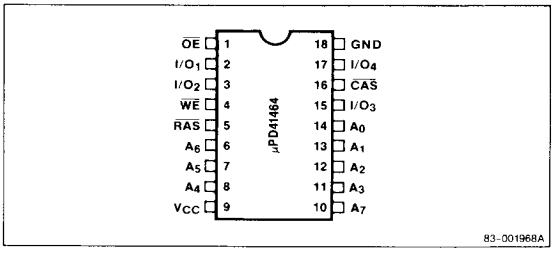
Refresh is accomplished by using $\overline{CAS}$ before $\overline{RAS}$ cycles, enabling the internal generation of the refresh address. Refresh can also be accomplished by using $\overline{RAS}$-only refresh or normal read or write cycles on the 256 address combinations of A_0-A_7 during the 4-ms refresh period.

Features

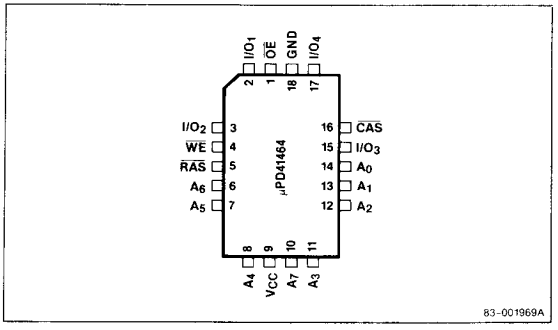
- ☐ 65,536-word by 4-bit organization
- ☐ Single +5-volt ±10% power supply
- ☐ $\overline{CAS}$ before $\overline{RAS}$ internal address refresh mode
- ☐ Multiplexed address inputs
- ☐ On-chip substrate bias generator
- ☐ Low power dissipation
  - — 28 mW (standby)
  - — 440 mW (active, $t_{RC} = t_{RC}$ min)
- ☐ Nonlatched TTL-compatible I/O
- ☐ Low input capacitance
- ☐ 256 refresh cycles during 4-ms period
- ☐ Standard plastic DIP, PLCC, and ZIP packages

Pin Configurations

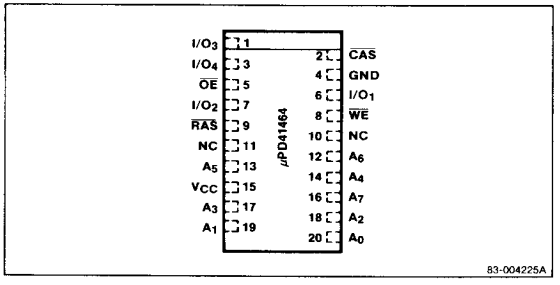
18-Pin Plastic DIP



18-Pin PLCC



20-Pin Plastic Zig-Zag Inline Package (ZIP)



Pin Identification

Symbol	Function
A_0-A_7	Address inputs
I/O_1-I/O_4	Data I/O
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
GND	Ground
V_{CC}	Power supply
NC	No connection

Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70 °C
Storage temperature, T_{STG}	−55 to +125 °C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	1 W

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Ordering Information

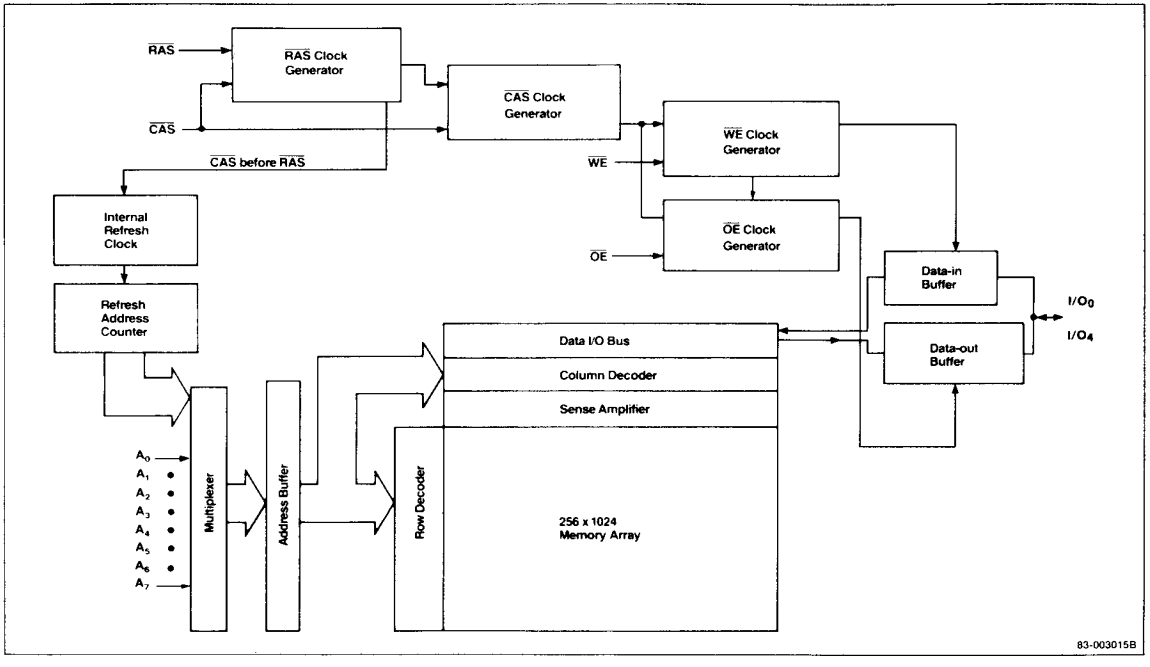
Part Number	Row Access Time (Max)	Package
μPD41464C-10	100 ns	18-pin plastic DIP
C-12	120 ns	
C-15	150 ns	
μPD41464L-10	100 ns	18-pin PLCC
L-12	120 ns	
L-15	150 ns	
μPD41464V-10	100 ns	20-pin ZIP
V-12	120 ns	
V-15	150 ns	

Capacitance

$T_A = 25\,°C$; $f = 1$ MHz

		Limits				
Parameter	Symbol	Min	Typ	Max	Unit	Pins Under Test
Input capacitance	C_{I1}			5	pF	A_0-A_7
Input capacitance	C_{I2}			8	pF	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$
Input/output capacitance	C_O			7	pF	I/O_1-I/O_4

Block Diagram



DC Characteristics

T_A = 0 to +70°C; V_{CC} = 5.0 V ±10%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Supply voltage	V_{CC}	4.5	5.0	5.5	V	Referenced to GND
Input voltage, high	V_{IH}	2.4		5.5	V	Referenced to GND
Input voltage, low	V_{IL}	−1.0		0.8	V	Referenced to GND
Standby current	I_{CC2}			5.0	mA	$\overline{RAS} = \overline{CAS} = V_{IH}$
Input leakage current	$I_{I(L)}$	−10		10	μA	V_{IN} = 0 to 5.5 V, all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	−10		10	μA	I/O is High-Z, $V_{I/O}$ = 0 to 5.5 V
Output voltage, low	V_{OL}	0		0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4		V_{CC}	V	I_{OH} = −5 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = 5.0 V ±10%

Parameter	Symbol	μPD41464-10 Min	Max	μPD41464-12 Min	Max	μPD41464-15 Min	Max	Unit	Test Conditions
Operating current, average	I_{CC1}		80		75		70	mA	$\overline{RAS}$, $\overline{CAS}$ cycling, $t_{RC} = t_{RC}$ min (Note 5)
Operating current, refresh mode, average	I_{CC3}		65		60		55	mA	$\overline{RAS}$ cycling, $\overline{CAS} = V_{IH}$, $t_{RC} = t_{RC}$ min (Note 5)
Operating current, page mode, average	I_{CC4}		55		50		45	mA	$\overline{RAS} = V_{IL}$, $\overline{CAS}$ cycling, $t_{PC} = t_{PC}$ min (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh mode, average	I_{CC5}		70		65		60	mA	$\overline{RAS}$ cycling, $\overline{CAS} = V_{IL}$, $t_{RC} = t_{RC}$ min (Note 5)
Random read or write cycle time	t_{RC}	200		220		260		ns	(Note 6)
Read-write cycle time	t_{RWC}	270		300		355		ns	(Note 6)
Page mode cycle time	t_{PC}	100		120		145		ns	(Note 6)
Refresh period	t_{REF}		4		4		4	ms	
Access time from $\overline{RAS}$	t_{RAC}		100		120		150	ns	(Notes 7, 8)
Access time from $\overline{CAS}$	t_{CAC}		50		60		75	ns	(Notes 7, 9)
Output buffer turn-off delay	t_{OFF}	0	25	0	30	0	40	ns	(Note 10)
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	(Note 3)
$\overline{RAS}$ precharge time	t_{RP}	90		90		100		ns	
$\overline{RAS}$ pulse width	t_{RAS}	100	10000	120	10000	150	10000	ns	
$\overline{RAS}$ hold time	t_{RSH}	50		60		75		ns	
$\overline{CAS}$ pulse width	t_{CAS}	50	10000	60	10000	75	10000	ns	
$\overline{CAS}$ hold time	t_{CSH}	100		120		150		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	25	60	25	75	ns	(Note 11)
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	(Note 12)
$\overline{CAS}$ precharge time, non-page cycle	t_{CPN}	25		25		25		ns	
$\overline{CAS}$ precharge time, page cycle	t_{CP}	40		50		60		ns	

AC Characteristics (cont)

Parameter	Symbol	μPD41464-10		μPD41464-12		μPD41464-15		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max		
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	0		0		0		ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		15		15		ns	
Column address setup time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		20		25		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	65		80		100		ns	
Read command setup time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		10		ns	(Note 13)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	(Note 13)
Write command hold time	t_{WCH}	25		30		40		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	75		90		115		ns	
Write command pulse width	t_{WP}	15		20		25		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	35		40		45		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	35		40		45		ns	
Data-in setup time	t_{DS}	0		0		0		ns	(Note 14)
Data-in hold time	t_{DH}	25		30		40		ns	(Note 14)
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	75		90		115		ns	
Write command setup time	t_{WCS}	0		0		0		ns	(Note 15)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	130		155		195		ns	(Note 15)
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	80		95		120		ns	(Note 15)
Access time from $\overline{OE}$	t_{OEA}		25		30		40	ns	
Data delay time	t_{OED}	25		30		40		ns	
$\overline{OE}$ command hold time	t_{OEH}	0		0		0		ns	
Output turn-off delay from $\overline{OE}$	t_{OEZ}	0	25	0	30	0	40	ns	
$\overline{OE}$ to $\overline{RAS}$ inactive setup time	t_{OES}	10		10		10		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh	t_{CHR}	20		25		30		ns	

Notes:

(1) An initial pause of 100 μs ($\overline{RAS}$ inactive) is required after power-up, followed by any 8 $\overline{RAS}$ cycles, before proper device operation is achieved.

(2) AC measurements assume $t_T = 5$ ns.

(3) V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.

(4) All voltages referenced to GND.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. For lot code K of μPD41464-15, t_{RC} min must be 270 ns and $I_{CC3} = 60$ mA.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range ($T_A = 0$ to $+70°C$) is assured. For lot code K of μPD41464-15, t_{RC} min must be 270 ns.

(7) Load = 2 TTL loads and 100 pF.

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} exceeds the value shown.

(9) Assumes that $t_{RCD} \geq t_{RCD}$ (max).

(10) t_{OFF} (max) and t_{OEZ} (max) define the time at which the outputs achieve the open circuit condition and are not referenced to V_{OH} or V_{OL}.

(11) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), access time is controlled exclusively by t_{CAC}.

(12) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

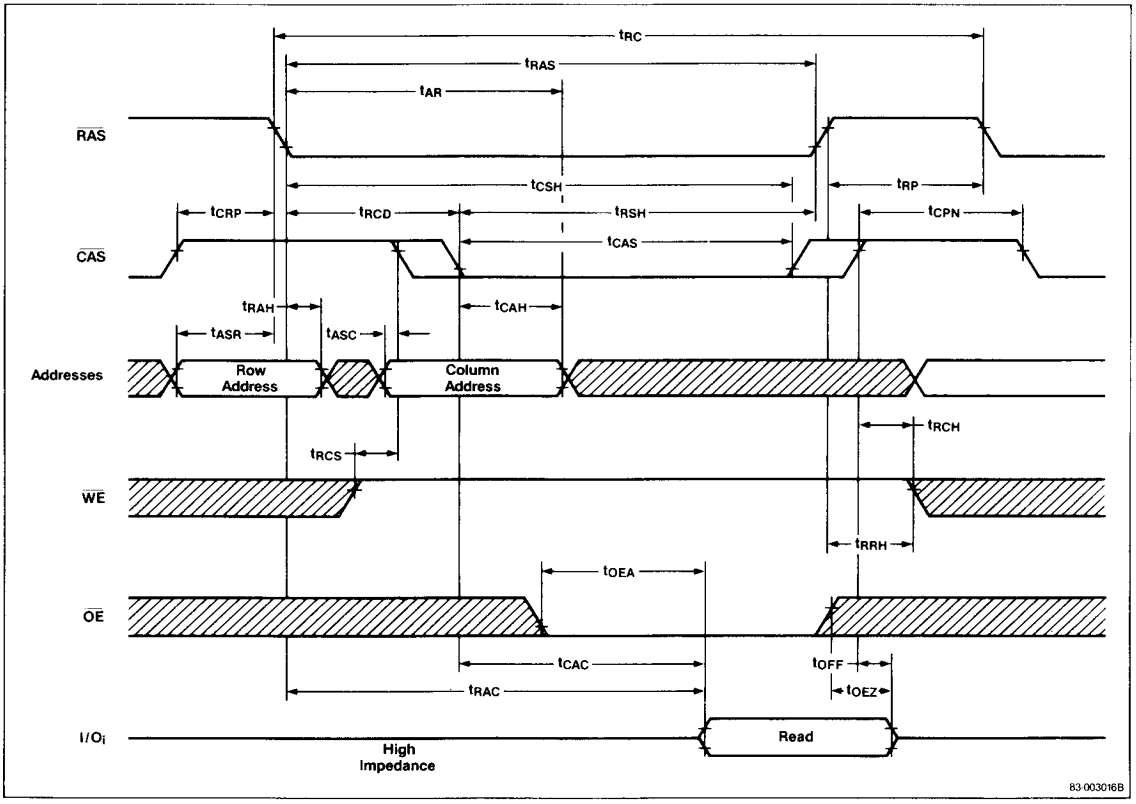
(13) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(14) These parameters are referenced to the leading edge of $\overline{CAS}$ for early write cycles and to the leading edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(15) t_{WCS}, t_{CWD}, and t_{RWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data I/O pins will remain high impedance throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and the data I/O pins will contain data read from the selected cells. If neither of the above conditions is met, the condition of the data I/O pins (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

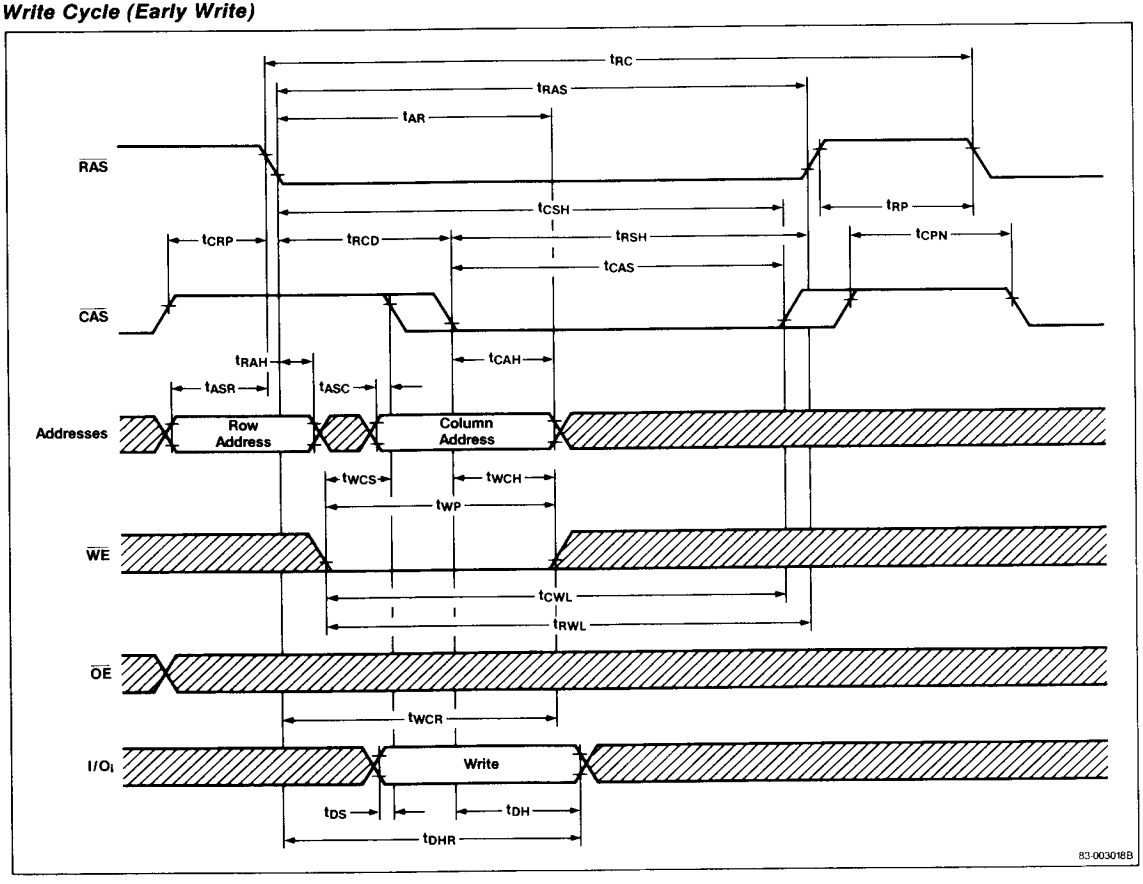
Timing Waveforms

Read Cycle



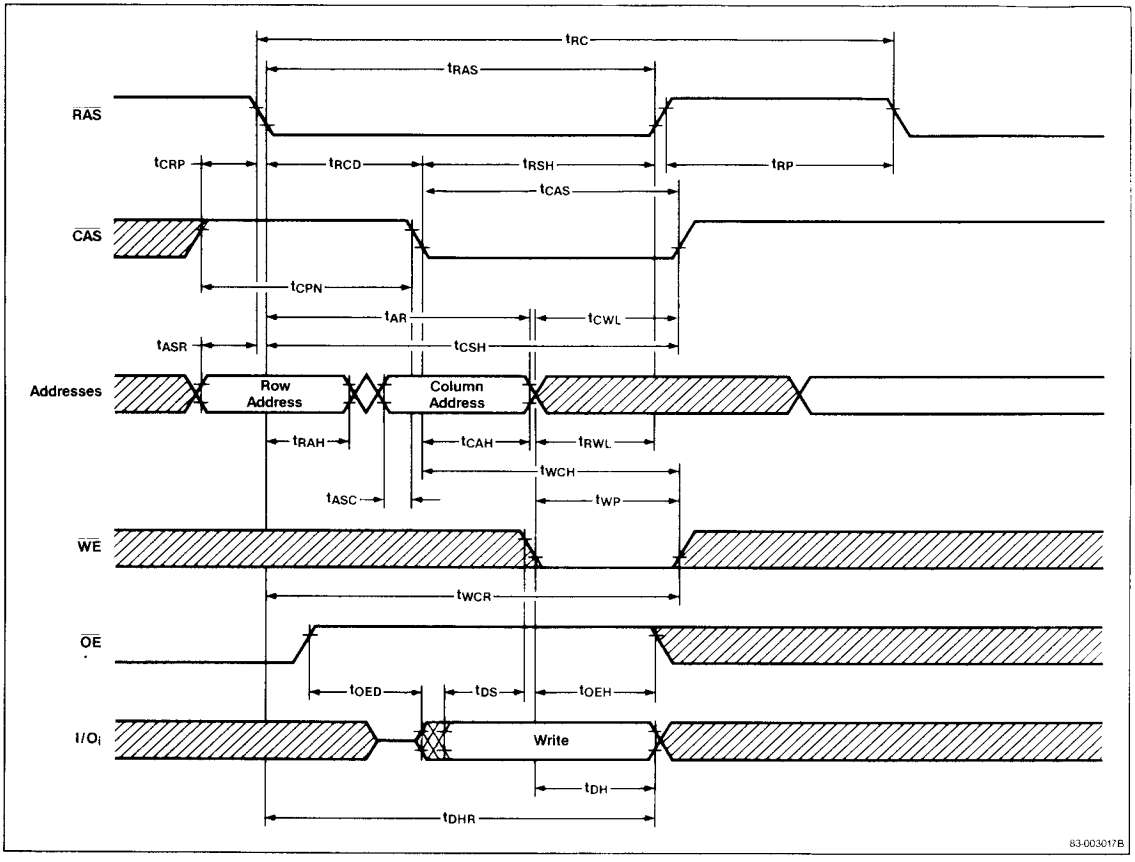
Timing Waveforms (cont)

Write Cycle (Early Write)



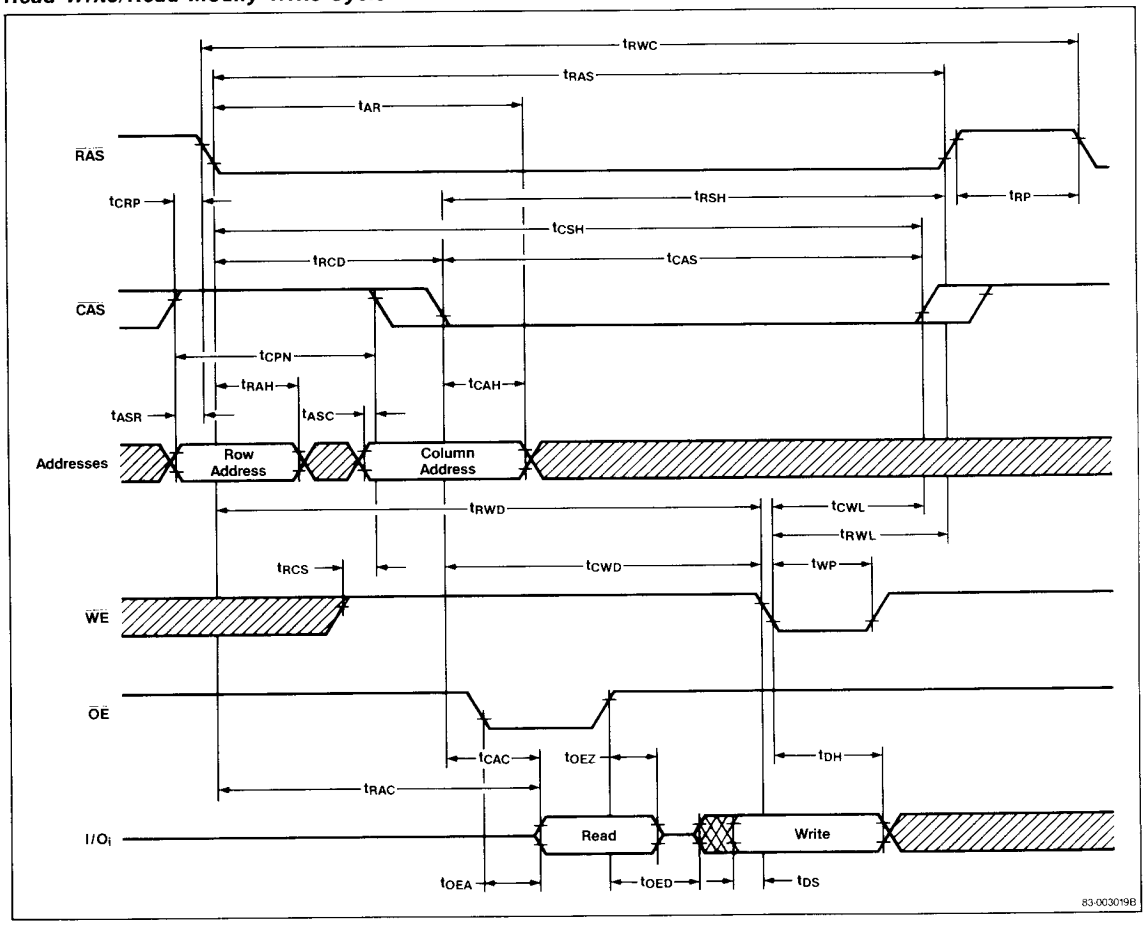
Timing Waveforms (cont)

$\overline{OE}$-Controlled Write Cycle



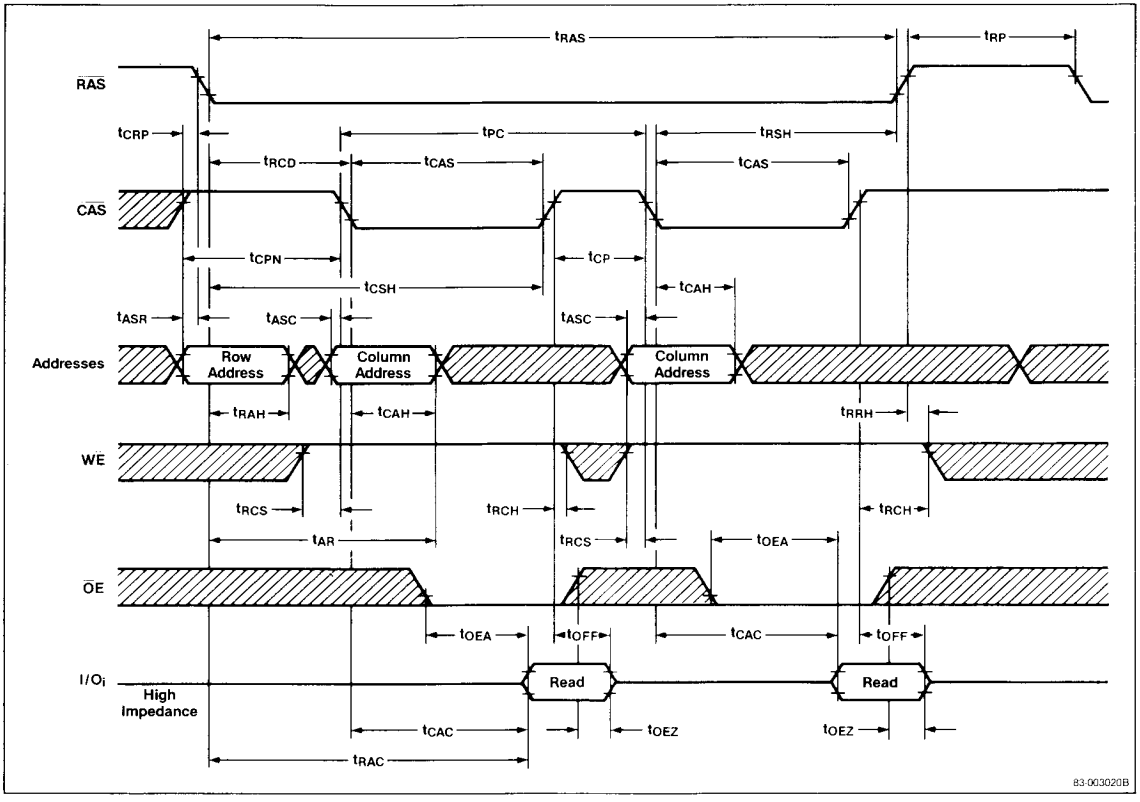
Timing Waveforms (cont)

Read-Write/Read-Modify-Write Cycle



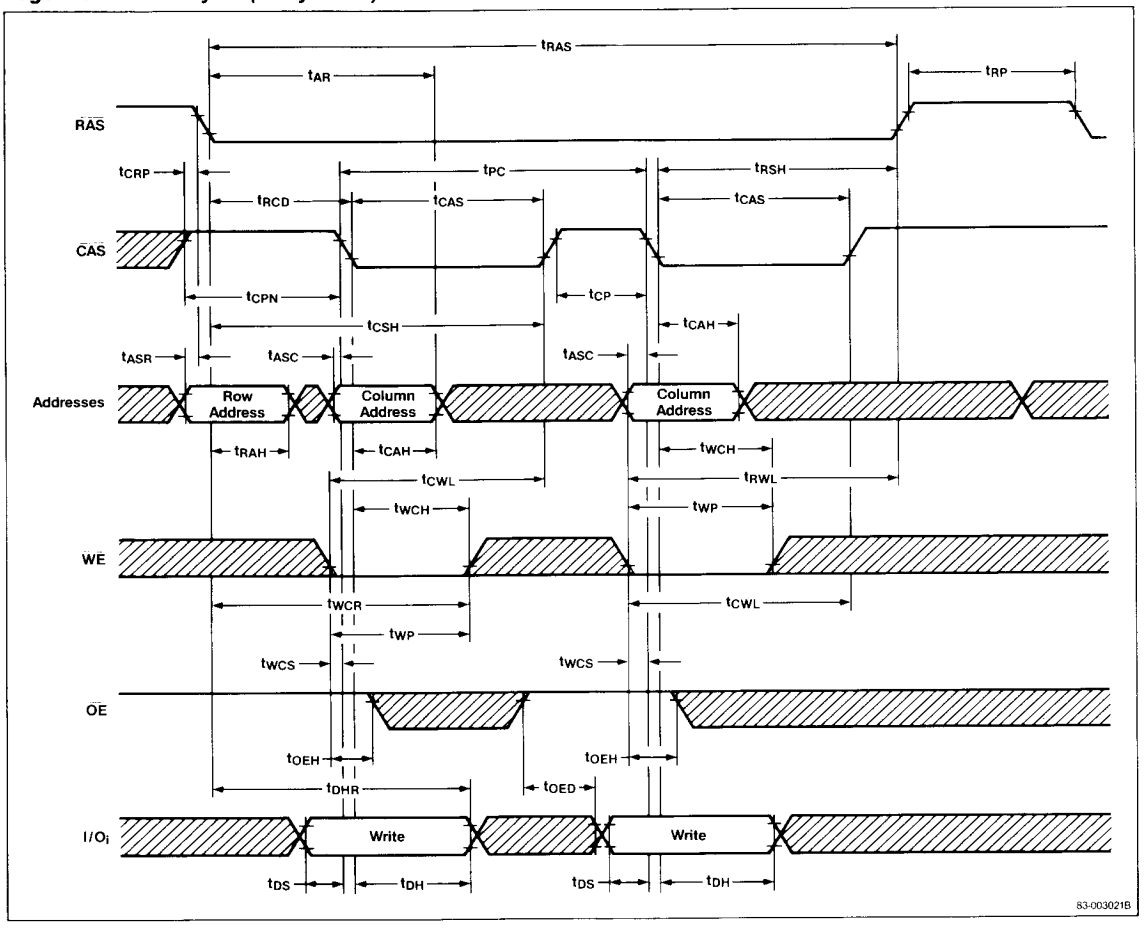
Timing Waveforms (cont)

Page Mode Read Cycle



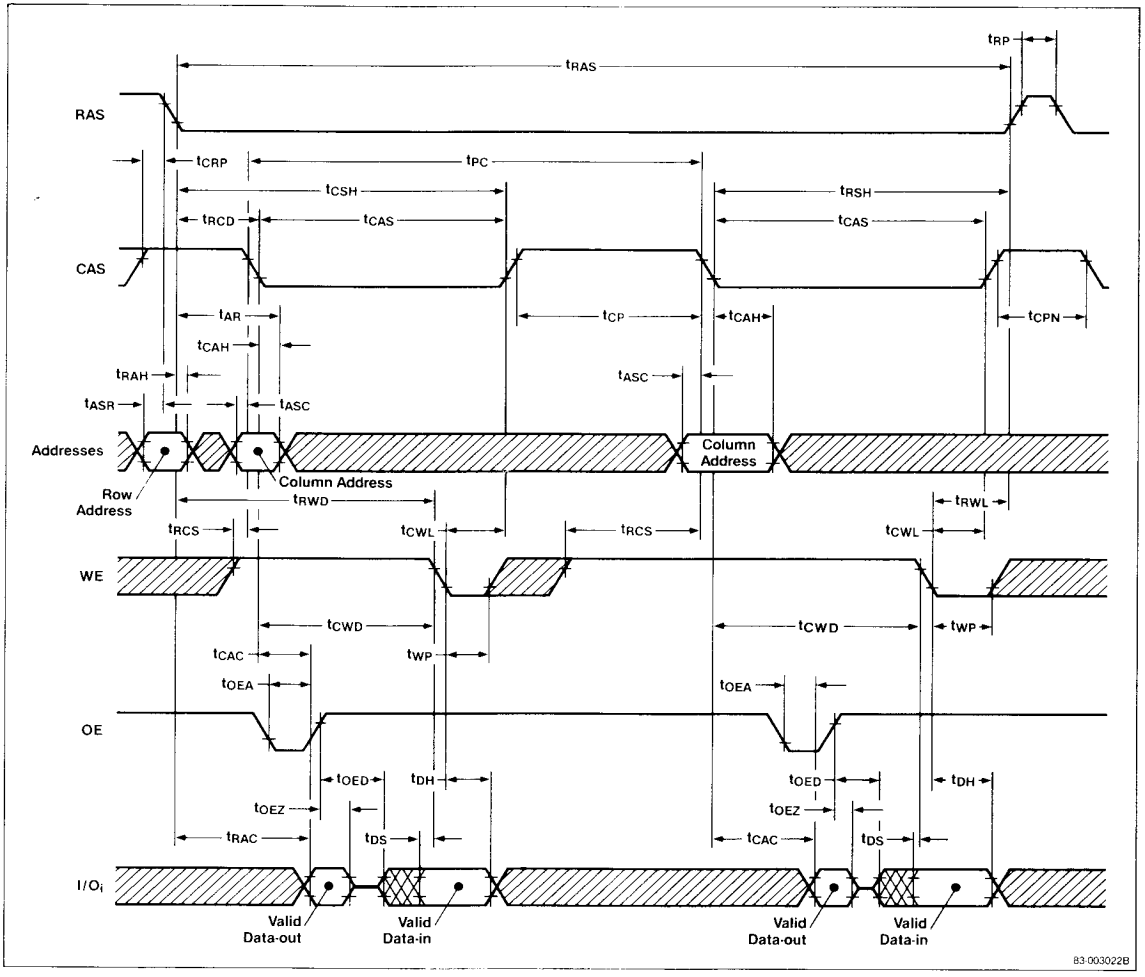
Timing Waveforms (cont)

Page Mode Write Cycle (Early Write)



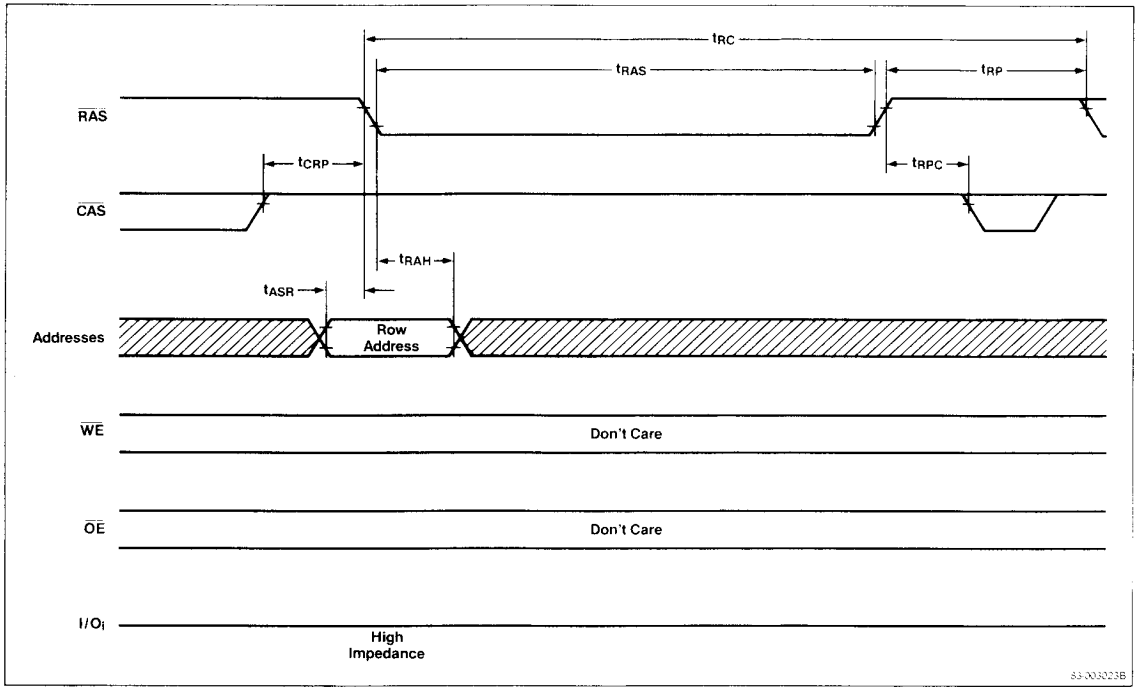
Timing Waveforms (cont)

Page Mode Read-Write/Read-Modify-Write Cycle



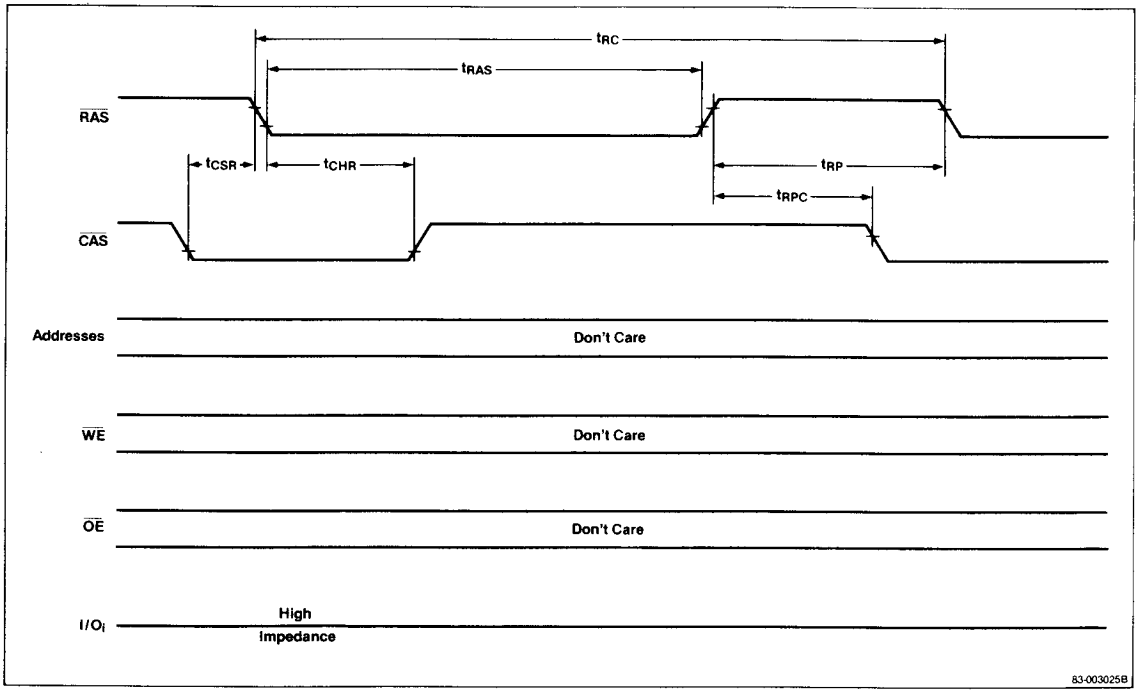
Timing Waveforms (cont)

$\overline{RAS}$-Only Refresh Cycle



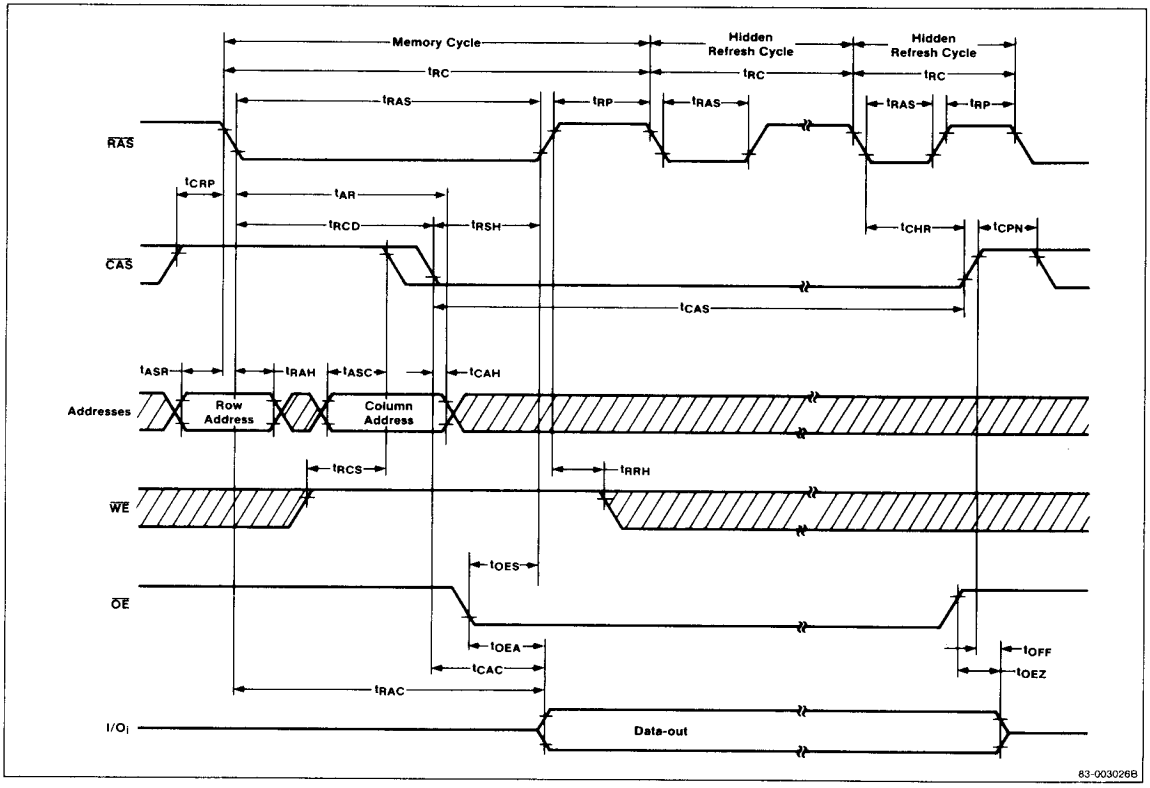
Timing Waveforms (cont)

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Timing Waveforms (cont)

Hidden Refresh Cycle



Package Drawings

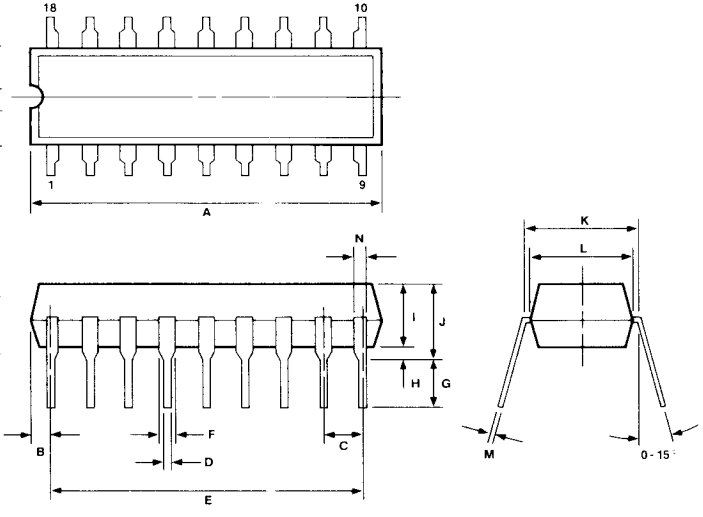
18-Pin Plastic DIP, μPD41464C (Semiwide Body, Process Codes L, F, and N)

Item	Millimeters	Inches
A	22.86 max	.900 max
B	1.27 max	.050 max
C	2.54 [TP]	.100 [TP]
D	.50 ± .10	.020 $^{+.004}_{-.005}$
E	20.32	.800
F	1.2 min	.047 min
G	3.2 ± .3	.126 ± .012
H	.51 min	.020 min
I	4.31 max	.170 max
J	5.08 max	.200 max
K	7.62 [TP]	.300 [TP]
L	6.7	.264
M	.25 $^{+.10}_{-.05}$	.010 $^{+.004}_{-.003}$
N	1.0 min	.039 min

Notes:

[1] Each lead centerline is located within .25 mm [.010 inch] of its true position [TP] at maximum material condition.

[2] Item "K" to center of leads when formed parallel.



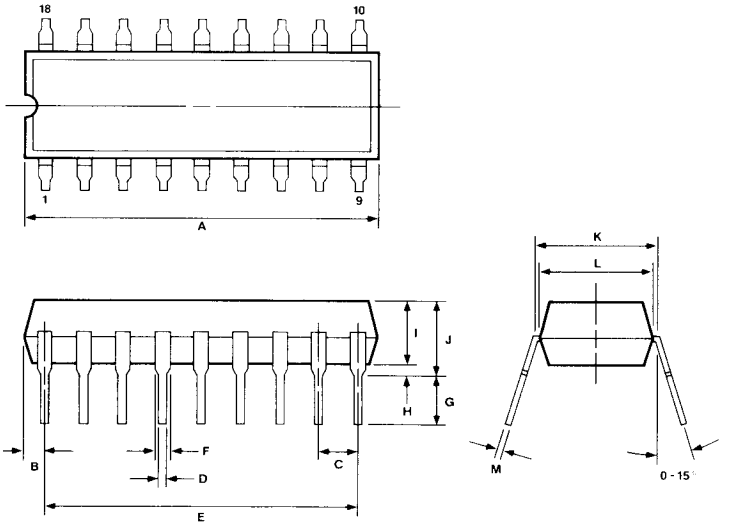
83-003588B

Package Drawings (cont)

18-Pin Plastic DIP (300-mil, Wide Body, Process Code K; superseded by Semiwide Body, Process Codes L, F, and N)

Item	Millimeters	Inches
A	22.86 max	.900 max
B	1.27 max	.050 max
C	2.54 [TP]	.100 [TP]
D	.50 ± .10	.020 $^{+.004}_{-.005}$
E	20.32	.800
F	1.2 min	.047 min
G	3.2 ± .3	.126 ± .012
H	.51 min	.020 min
I	4.31 max	.170 max
J	5.08 max	.200 max
K	7.62 [TP]	.300 [TP]
L	7.35	.289
M	.25 $^{+.10}_{-.05}$	.010 $^{+.004}_{-.003}$

Notes:
[1] Each lead centerline is located within .25 mm [.010 inch] of its true position [TP] at maximum material condition.
[2] Item "K" to center of leads when formed parallel.



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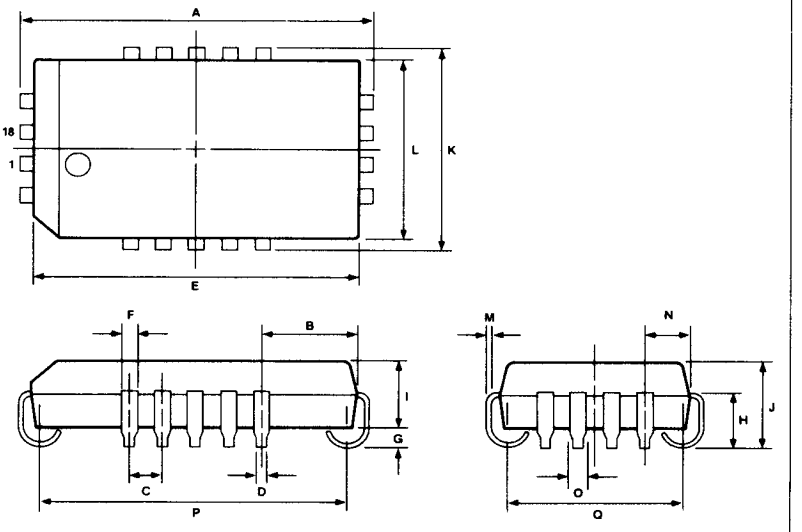
Package Drawings (cont)

18-Pin PLCC, μPD41464L

Item	Millimeters	Inches
A	13.4 ± .20	.528 ± .008
B	3.71 ± .15	.146 ± .006
C	1.27	.050
D	.40 ± .10	.016 ± .004
E	12.5	.492
F	.60	.024
G	.8 min	.031 min
H	2.40 ± .20	.094 ± .008
I	2.6	.102
J	3.50 ± .20	.138 ± .008
K	8.30 ± .20	.327 ± .008
L	7.40	.291
M	.20 $^{+.10}_{-.05}$	.008 $^{+.004}_{-.002}$
N	1.80 ± .20	.071 ± .008
O	.70	.028
P	11.68 ± .20	.460 ± .008
Q	6.6 ± .20	.260 ± .008

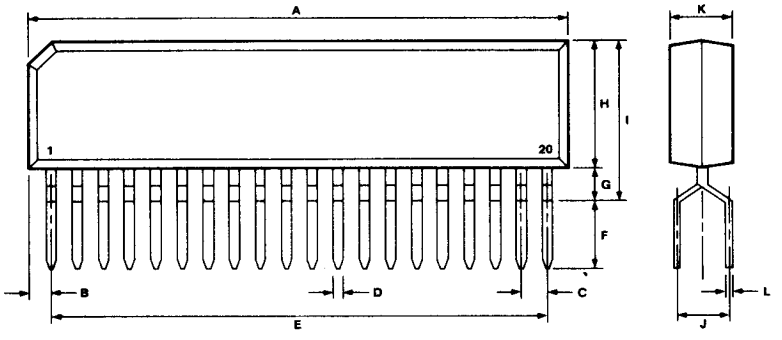


Package Drawings (cont)

20-Pin Plastic Zig-Zag Inline Package (ZIP)

Item	Millimeters	Inches
A	26.00 max	1.024 max
B	1.27 max	.050 max
C	1.27 [TP]	.050 [TP]
D	.50 ± .10	$.020^{+.004}_{-.005}$
E	24.13	.950
F	3.00 min	.118 min
G	.9 min	.035 min
H	6.60	.260
I	8.26 max	.325 max
J	2.54 [TP]	.100 [TP]
K	2.8 ± .2	.110 ± .008
L	$.25^{+.10}_{-.05}$	$.010^{+.004}_{-.003}$

Note:
[1] Each lead centerline is located within .12 mm [.005 inch] of its true position [TP] at maximum material condition.



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