μPD7537A/38A/75CG38E 4-Bit, Single-Chip CMOS Microcomputers With FIP® Driver

Description

The μPD7537A, μPD7538A, and μPD75CG38E are 4-bit, single-chip CMOS microcomputers with the μPD7500 architecture and FIP direct-drive capability.

The μPD7537A contains a 2048 × 8-bit ROM and a 128 × 4-bit RAM. The μPD7538A contains a 4096 × 8-bit ROM and a 160 × 4-bit RAM.

The μPD7537A/38A contains two 4-bit general purpose registers located outside RAM. The subroutine stack is implemented in RAM for greater depth and flexibility. The μPD7537A/38A typically executes 67 instructions with a 5 μs instruction cycle time.

The μPD7537A/38A has one external and two internal edge-triggered hardware-vectored interrupts. An 8-bit timer/event counter and an 8-bit serial interface help to reduce software requirements.

Thirty-one high-voltage lines are organized into the 3-bit output port 2, the 4-bit output ports 3, 8, and 9, and the 4-bit I/O ports 4, 5, 10, and 11.

The low power consumption CMOS process allows the use of a power supply between 2.7 V and 6.0 V. Current consumption is less than 3.0 mA maximum, and can be further reduced in the halt and stop power-down modes.

The μPD75CG38E is a piggyback EPROM version of the μPD7537A/38A. Pin-compatible and function-compatible with the final, masked versions of the μPD7537A/38A, the μPD75CG38E is used for prototyping and for aiding in program development.

Features

- ☐ 67 instructions
- ☐ Instruction cycle:
  - — Internal clock: 3.3 μs/600 kHz, 5 V
  - — External clock: 3.3 μs/600 kHz, 5 V
- ☐ Upwardly compatible with the μPD7500 series product family
- ☐ 4,096 × 8-bit ROM (μPD7538A/75CG38E)
  2,048 × 8-bit ROM (μPD7537A)
- ☐ 160 × 4-bit RAM (μPD7538A/75CG38E)
  128 × 4-bit RAM (μPD7537A)
- ☐ 35 I/O lines
- ☐ 31 high-voltage output lines that can directly drive a vacuum fluorescent diplay (FIP)
- ☐ Can select either a pull-down resistor or open-drain output per 31 high-voltage outputs (mask optional)
- ☐ Vectored interrupts: one external, two internal
- ☐ 8-bit timer/event counter
- ☐ 8-bit serial interface
- ☐ Standby function (HALT, STOP)
- ☐ Data retention mode
- ☐ Zero-cross detector on $P0_0$/INT0 input (mask optional)
- ☐ System clock (μPD7537A/7538A/75CG38E): on-chip ceramic oscillator
- ☐ CMOS technology
- ☐ Low power consumption
- ☐ Single power supply
  - — μPD7537A/7538A: 2.7 V to 6.0 V
  - — μPD75CG38E: 5.0 V ± 10%

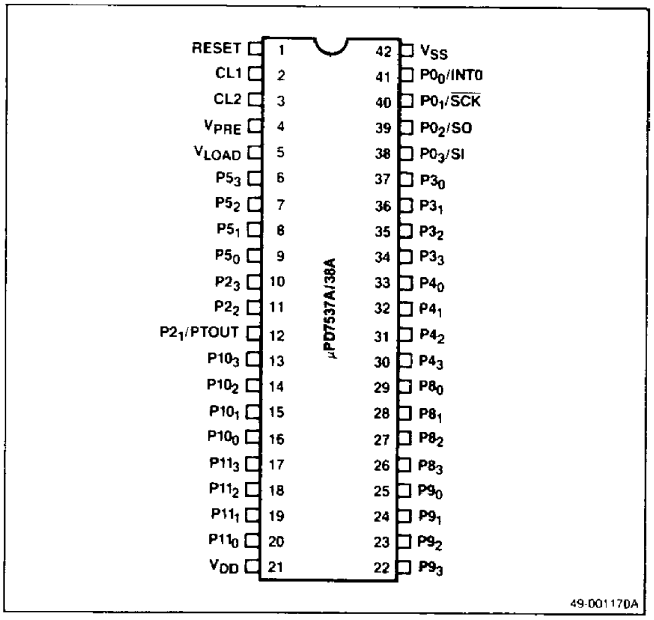
FIP is the registered trademark for NEC's fluorescent indicator panel (vacuum fluorescent display).

Ordering Information

Part Number	Package Type	Max Frequency of Operation
μPD7537AC / 38AC	42-pin plastic DIP	610 kHz
μPD7537ACU / 38ACU	42-pin plastic shrink DIP	610 kHz
μPD75CG38E	42-pin ceramic piggyback DIP	500 kHz

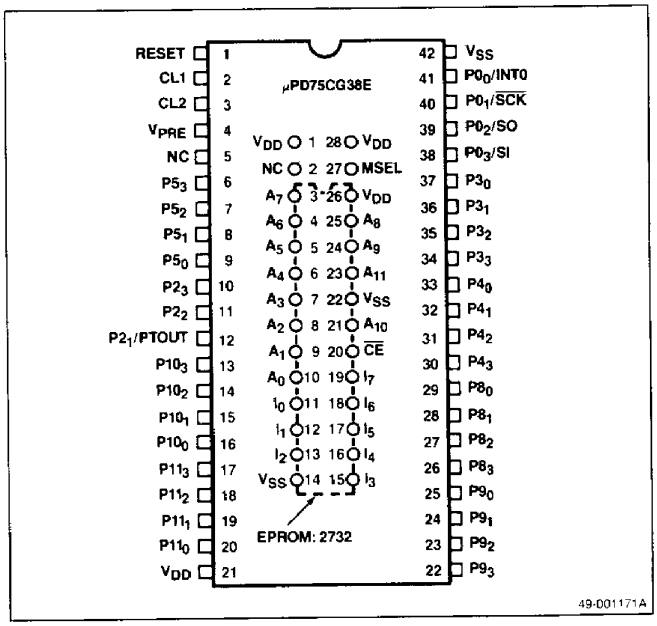
Pin Configurations

μPD7537A/38A 42-Pin Plastic DIP or Shrink DIP



Pin Configurations (cont)

μPD75CG38E 42-Pin Ceramic Piggyback DIP



Pin Identification

μPD7537A/38A and μPD75CG38E

No.	Symbol	Function
1	RESET	Reset input
2, 3	CL1, CL2	Clock pins
4	V_{PRE}	High-voltage output predriver supply
5	V_{LOAD}	High-voltage output option resistor supply 7537A/38A only
6-9	$P5_0$-$P5_3$	High-voltage I/O port 5
10, 12	$P2_3$, $P2_2$ $P2_1$/PTOUT	High-voltage output port 2, and output port from timer/event counter (PTOUT)
13-16	$P10_0$-$P10_3$	High-current, high-voltage I/O port 10
17-20	$P11_0$-$P11_3$	High-voltage, high-current I/O port 11
21	V_{DD}	Positive power supply
22-25	$P9_0$-$P9_3$	High-voltage, high-current output port 9
26-29	$P8_0$-$P8_3$	High-voltage, high-current output port 8
30-33	$P4_0$-$P4_3$	High-voltage I/O port 4
34-37	$P3_0$-$P3_3$	High-voltage output port 3
38	$P0_3$/SI	4-bit input of port 0; or serial data input
39	$P0_2$/SO	(SI), serial data output (SO), serial clock
40	$P0_1$/$\overline{SCK}$	I/O ($\overline{SCK}$), and external interrupt input
41	$P0_0$/INT0	(INT0) or zero-cross detect input ($P0_0$).
42	V_{SS}	Ground

μPD75CG38E EPROM

No.	Symbol	Function
1	V_{DD}	Connection to pin 21 of μPD75CG38E
2	NC	No connection
3-10, 21, 24, 25	A_0-A_{10}	EPROM address output
11-13, 15-19	I_0-I_7	Data read input from the EPROM
14	V_{SS}	Connection to EPROM GND pin
20	$\overline{CE}$	Chip enable output
22	V_{SS}	Supplies EPROM OE signal
23	A_{11}	Program counter MSB output
26	V_{DD}	Supplies V_{CC} to the EPROM
27	MSEL	Mode select input
28	V_{DD}	Supplies high-level signal to MSEL

Note:

(1) Output drivers on ports 2-5 and 8-11 are mask-optional. Accordingly, either an open-drain output or a pull-down resistor can be selected. V_{LOAD} is suitable for an output driver with a pull-down resistor.

(2) Ports 2-5 are suitable as FIP segment signal outputs, and ports 8-11 are suitable for FIP digit signal outputs.

(3) Ports 8-11 have high-current drive capability and can drive an LED directly.

Pin Functions, μPD7537A/38A and μPD75CG38E

RESET

System reset (input).

CL1, CL2

Connection to the ceramic oscillator. CL1 is the external clock input.

V_{PRE}

Negative power supply for high-voltage output predrivers (for ports 2-5, 8-11).

V_{LOAD}

Negative power supply for optional load resistors (pull-down resistors) of high-voltage output drivers (for ports 2-5, 8-11). This pin is only on the μPD7537A/38A.

$P5_3$-$P5_0$

4-bit, high-voltage I/O port 5.

$P2_1$-$P2_3$

3-bit, high-voltage output port 2.

PTOUT

Output port for the timer/event counter.

$P10_3$-$P10_0$

4-bit, high-voltage, high-current I/O port 10. Capable of bit set/reset by SPBL/RPBL instructions.

$P11_3$-$P11_0$

4-bit, high-voltage, high-current I/O port 11. Capable of bit set/reset by SPBL/RPBL instructions.

V_{DD}

Positive power supply.

$P9_3$-$P9_0$

4-bit, high-voltage, high-current output port 9. Capable of bit set/reset by SPBL/RPBL instructions.

$P8_3$-$P8_0$

4-bit, high-voltage, high-current output port 8. Capable of bit set/reset by SPBL/RPBL instructions.

$P4_3$-$P4_0$

4-bit, high-voltage I/O port 4.

$P3_3$-$P3_0$

4-bit, high-voltage output port 3.

$P0_0$-$P0_3$

4-bit input port 0. $P0_0$ is also used as the zero-cross detection input.

SI

Serial data input.

SO

Serial data output.

$\overline{SCK}$

Serial I/O clock.

INT0

External interrupt input.

V_{SS}

Ground.

Pin Functions, μPD75CG38E EPROM

MSEL

Changes the addressing area of the external EPROM and the on-chip RAM (with a pull-down resistor). Connecting a jumper between socket pins 27 (MSEL) and 28 (V_{DD}) selects μPD7537A mode (2-Kbyte EPROM, 128 × 4-bit RAM). Leaving MSEL open selects μPD7538A mode (4-Kbyte EPROM, 160 × 4-bit RAM).

A_0-A_{10}

Output the low-order 11 bits of the program counter (PC_0-PC_{10}). Used as EPROM address signals.

A_{11}

When MSEL is high level, A_{11} outputs high-level signals. When MSEL is open, A_{11} outputs the MSB of the PC, which is used as the most significant address signal of the 4-Kbyte EPROM 2732.

I_0-I_7

Input data read from the EPROM.

$\overline{CE}$

Outputs the chip enable signal to the EPROM.

V_{DD}

Pin 26 is electrically equivalent to the bottom V_{DD} pin and is used to supply V_{CC} to the EPROM. Pin 28 is electrically equivalent to the bottom V_{DD} pin and is used to supply the high level signal to MSEL. Pin 1 connects to pin 21 of μPD75CG38E.

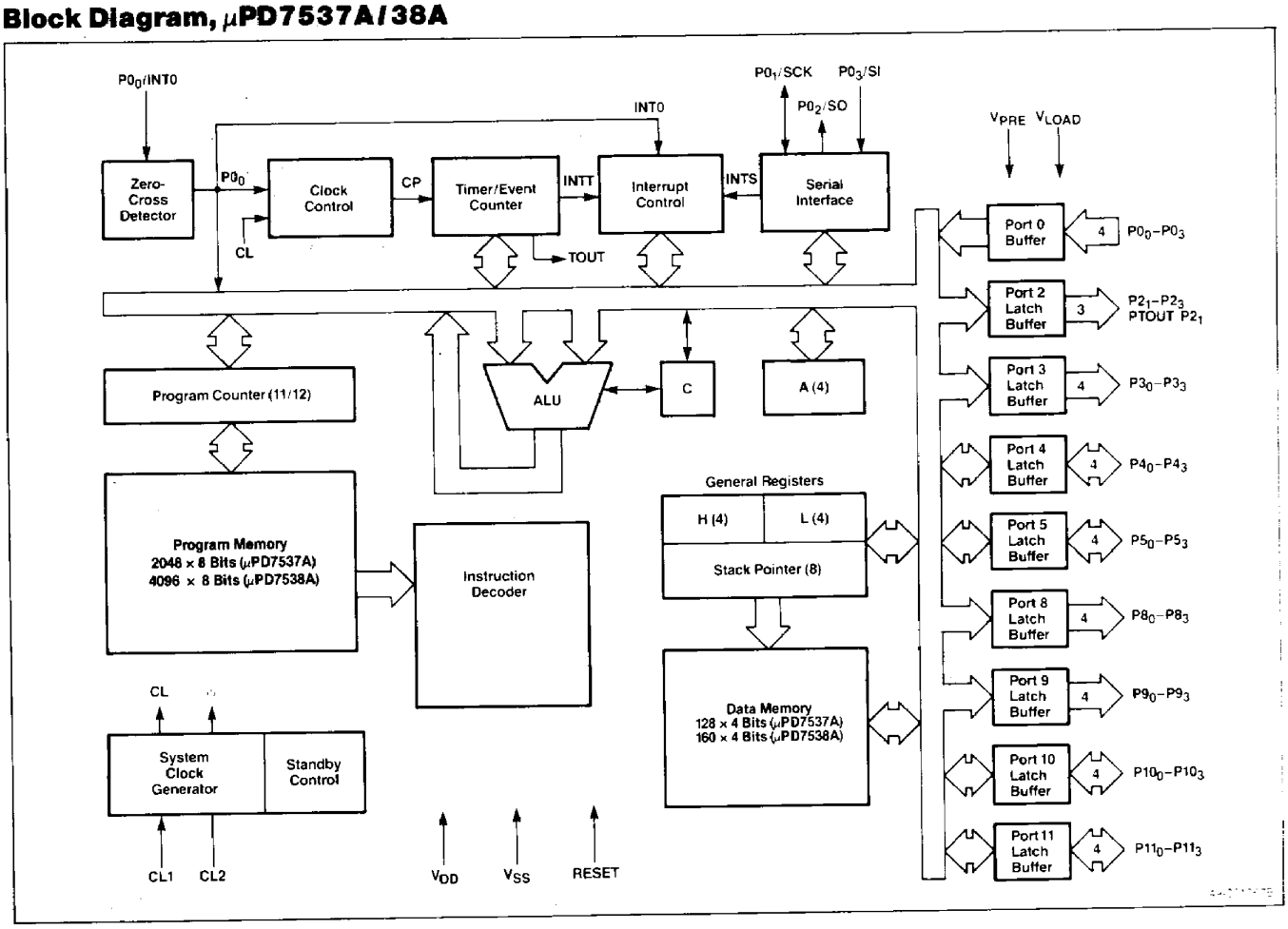
V_{SS}

Pin 14 is electrically equivalent to the bottom V_{SS} pin in voltage, and is connected to the EPROM GND pin. Pin 22 is electrically equivalent to the bottom V_{SS} pin and is used to supply the OE signal to the EPROM.

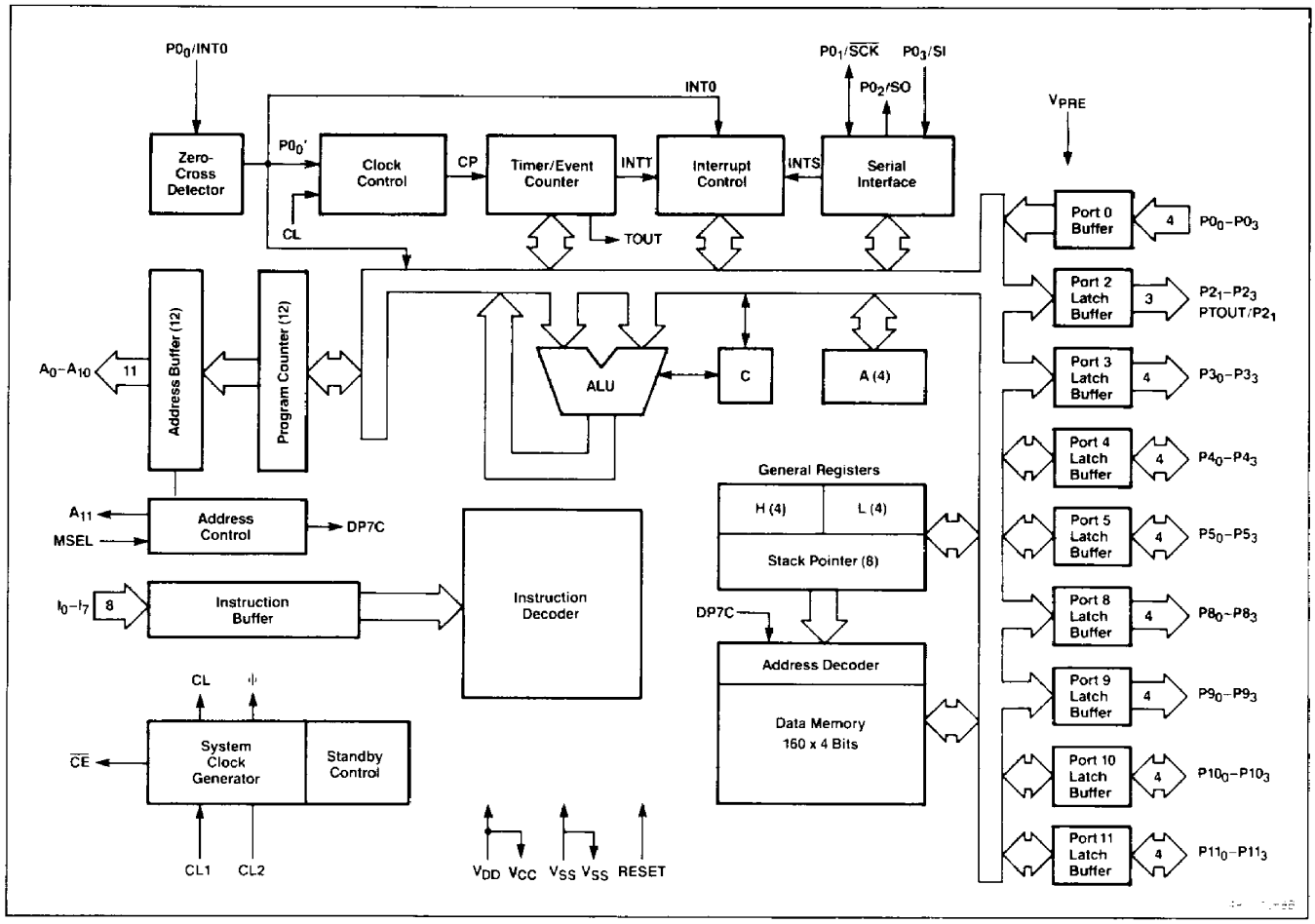
Instruction Set

Refer to the User's Manual. The instruction set appears also as subset A4 in the data sheet for the μPD7500 series of single-chip microcomputers.

Block Diagram, μPD7537A/38A



Block Diagram, μPD75CG38E



Absolute Maximum Ratings

$T_A = 25°C$

Power supply voltage, V_{DD}	−0.3 V to +7 V
Power supply voltage, V_{LOAD} (μPD7537A / 38A)	V_{DD} − 40 V to V_{DD} +0.3 V
Power supply voltage, V_{PRE}	V_{DD} − 12 V to V_{DD} +0.3 V
Input voltage, except ports 4, 5, 10, 11, V_{IN}	−0.3 V to V_{DD} +0.3 V
Input voltage, ports 4, 5, 10, 11, V_{IN}	V_{DD} − 40 V to V_{DD} +0.3 V
Output voltage, except ports 2–5, 8–11, V_O	−0.3 V to V_{DD} +0.3 V
Output voltage, ports 2–5, 8–11, V_O	V_{DD} − 40 V to V_{DD} +0.3 V
Output current high, per pin: $P0_1$, $P0_2$; I_{OH}	−15 mA
Output current high, per pin: ports 2–5, 8–11; I_{OH}	−30 mA
Output current high, ports 3, 4, 8, 9 total, I_{OH}	−55 mA
Output current high, ports 2, 5, 10, 11 total, I_{OH}	−55 mA
Output current low, per pin, I_{OL}	15 mA
Output current low, all ports total, I_{OL}	15 mA
Operating temperature, T_{OPT}	−10°C to +70°C
Storage temperature, T_{STG}	−65°C to +150°C

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of the specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

$T_A = 25°C$, $V_{DD} = 0$ V, f = 1.0 MHz, Unmeasured pins returned to GND

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_I			15	pF	$P0_0$–$P0_3$
Output capacitance	C_O			15	pF	Port 2
				35	pF	Ports 3, 8, 9
I/O capacitance	C_{IO}			15	pF	$P0_1$, $P0_2$
				35	pF	Ports 4, 5, 10, 11

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DC Characteristics

μPD7537A/38A

$T_A = -10°C$ to $+70°C$, $V_{DD} = +2.7$ V to 6.0 V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input voltage, low	V_{IL1}	0		0.3 V_{DD}	V	Port 0, RESET
	V_{IL2}	0		0.5	V	CL1
	V_{IL3}	$V_{DD}-35$		0.3 V_{DD}	V	Ports 4, 5, 10, 11
Input voltage, high	V_{IH1}	0.7 V_{DD}		V_{DD}	V	Port 0, RESET
	V_{IH2}	$V_{DD}-0.5$		V_{DD}	V	CL1
	V_{IH3}	0.7 V_{DD}		V_{DD}	V	Ports 4, 5, 10, 11; $4.5\,V \leq V_{DD} \leq 6.0\,V$
		$V_{DD}-0.5$		V_{DD}	V	Ports 4, 5, 10, 11; $2.7\,V \leq V_{DD} < 4.5\,V$
Output voltage, low	V_{OL}			0.4	V	PO_1, PO_2; $4.5\,V \leq V_{DD} \leq 6.0\,V$; $I_{OL} = 1.6$ mA
				0.5	V	PO_1, PO_2; $I_{OL} = 400\,\mu A$
Output voltage, high	V_{OH}	$V_{DD}-2.0$			V	Ports 2–5, $I_{OH} = -4$ mA (Note 1)
		$V_{DD}-2.0$			V	Ports 8–11, $I_{OH} = -10$ mA (Note 1)
		$V_{DD}-2.0$			V	Ports 2–5, $I_{OH} = -2$ mA (Note 2)
		$V_{DD}-2.0$			V	Ports 8–11, $I_{OH} = -5$ mA (Note 2)
		$V_{DD}-1.0$			V	PO_1, PO_2; $I_{OH} = -1$ mA (Note 3)
		$V_{DD}-0.5$			V	PO_1, PO_2; $I_{OH} = -100\,\mu A$
Input leakage current, low	I_{LIL1}			−3	μA	$V_{IN} = 0$ V; $P0_0$–$P0_3$ (Note 4)
	I_{LIL2}			−40	μA	$V_{IN} = 0$ V; $P0_0$ (Note 5)
	I_{LIL3}			−20	μA	$V_{IN} = 0$ V; CL1
	I_{LIL4}			−10	μA	$V_{IN} = V_{DD} - 35$ V; ports 4, 5, 10, 11
Input leakage current, high	I_{LIH1}			3	μA	$V_{IN} = V_{DD}$; $P0_0$ (Note 4)–$P0_3$
	I_{LIH2}			40	μA	$V_{IN} = V_{DD}$; $P0_0$ (Note 5)
	I_{LIH3}			20	μA	$V_{IN} = V_{DD}$; CL1
	I_{LIH4}			80	μA	$V_{IN} = V_{DD}$; ports 4, 5, 10, 11
Output leakage current, low	I_{LOL1}			−3	μA	$V_O = 0$ V; PO_1, PO_2
	I_{LOL2}			−10	μA	$V_O = V_{DD} - 35$ V; ports 2–5, 8–11
Output leakage current, high	I_{LOH1}			3	μA	$V_O = V_{DD}$; except ports 4, 5, 10, 11
	I_{LOH2}			80	μA	$V_O = V_{DD}$; ports 4, 5, 10, 11
Supply current, normal operation	I_{DD1}		1.5	4.0	mA	$V_{DD} = 5\,V \pm 10\%$, $f_{CC} = 600$ kHz
Supply current, HALT mode (Note 6)	I_{DD2}		700	1800	μA	$V_{DD} = 5\,V \pm 10\%$, $f_{CC} = 600$ kHz (Note 4)
			230	700	μA	$V_{DD} = 3\,V \pm 10\%$, $f_{CC} = 600$ kHz (Note 4)
			710	1840	μA	$V_{DD} = 5\,V \pm 10\%$, $f_{CC} = 600$ kHz (Note 5)
			237	730	μA	$V_{DD} = 3\,V \pm 10\%$, $f_{CC} = 600$ kHz (Note 5)
Supply current, STOP mode (Note 6)	I_{DD3}		0.1	10	μA	(Notes 4, 6)
			10	40	μA	$V_{DD} = 5\,V \pm 10\%$ (Note 5)
			7	30	μA	$V_{DD} = 3$ V (Note 5)

Note:

(1) $V_{PRE} = V_{DD} - 9\,V \pm 1\,V$. The circuit in figure 5 is recommended.

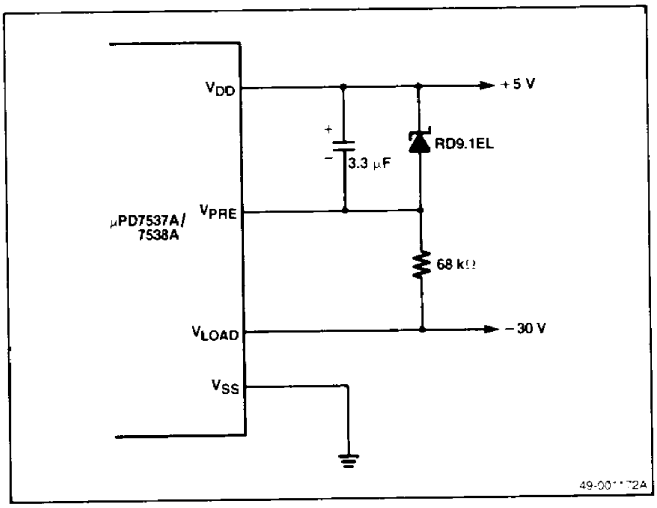
(2) $V_{PRE} = 0$ V. $V_{DD} = 4.5$ V to 6.0 V.

(3) $V_{DD} = 4.5$ V to 6.0 V.

(4) Without zero-cross detector.

(5) With zero-cross detector.

Figure 1. Recommended Circuit, μPD7537A/7538A



DC Characteristics (cont)

μPD75CG38E

$T_A = -10°C$ to $+70°C$, $V_{DD} = +5\,V \pm 10\%$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input voltage, low	V_{IL1}	0		$0.3\,V_{DD}$	V	Port 0, RESET
	V_{IL2}	0		0.5	V	CL1
	V_{IL3}	$V_{DD}-35$		$0.3\,V_{DD}$	V	Ports 4, 5, 10, 11
Input voltage, high	V_{IH1}	$0.7\,V_{DD}$		V_{DD}	V	Port 0, RESET
	V_{IH2}	$V_{DD}-0.5$		V_{DD}	V	CL1
	V_{IH3}	$0.7\,V_{DD}$		V_{DD}	V	Ports 4, 5, 10, 11
Output voltage, low	V_{OL}			0.4	V	PO_1, PO_2; $I_{OL} = 1.6$ mA
				0.5	V	PO_1, PO_2; $I_{OL} = 400\,\mu A$
Output voltage, high	V_{OH}	$V_{DD}-2.0$			V	Ports 2–5, $I_{OH} = -4$ mA (Note 1)
		$V_{DD}-2.0$			V	Ports 8–11, $I_{OH} = -10$ mA (Note 1)
		$V_{DD}-2.0$			V	Ports 2–5, $I_{OH} = -2$ mA (Note 2)
		$V_{DD}-2.0$			V	Ports 8–11, $I_{OH} = -5$ mA (Note 2)
		$V_{DD}-1.0$			V	PO_1, PO_2; $I_{OH} = -1$ mA (Note 2)
Input current, low (I_0–I_7)	I_{IL}			−200	μA	$V_{IN} = 0$ V
Input current, high (MSEL)	I_{IH}			300	μA	$V_{IN} = V_{DD}$
Input leakage current, low	I_{LIL1}			−3	μA	$V_{IN} = 0$ V; PO_1–PO_3
	I_{LIL2}			−40	μA	$V_{IN} = 0$ V; PO_0
	I_{LIL3}			−20	μA	$V_{IN} = 0$ V; CL1
	I_{LIL4}			−10	μA	$V_{IN} = V_{DD} - 35$ V; ports 4, 5, 10, 11
Input leakage current, high	I_{LIH1}			3	μA	$V_{IN} = V_{DD}$; PO_1–PO_3
	I_{LIH2}			40	μA	$V_{IN} = V_{DD}$; PO_0
	I_{LIH3}			20	μA	$V_{IN} = V_{DD}$; CL1
	I_{LIH4}			80	μA	$V_{IN} = V_{DD}$; ports 4, 5, 10, 11
Output leakage current, low	I_{LOL1}			−3	μA	$V_O = 0$ V; PO_1, PO_2
	I_{LOL2}			−10	μA	$V_O = V_{DD} - 35$ V; ports 2–5, 8–11
Output leakage current, high	I_{LOH1}			3	μA	$V_O = V_{DD}$; except ports 4, 5, 10, 11
	I_{LOH2}			80	μA	$V_O = V_{DD}$; ports 4, 5, 10, 11
Supply current, normal operation	I_{DD1}		1.0	3.0	mA	$f_{CC} = 400$ kHz
Supply current, HALT mode (Note 3)	I_{DD2}		460	1230	μA	$f_{CC} = 400$ kHz
Supply current, STOP mode (Note 3)	I_{DD3}		10	40	μA	

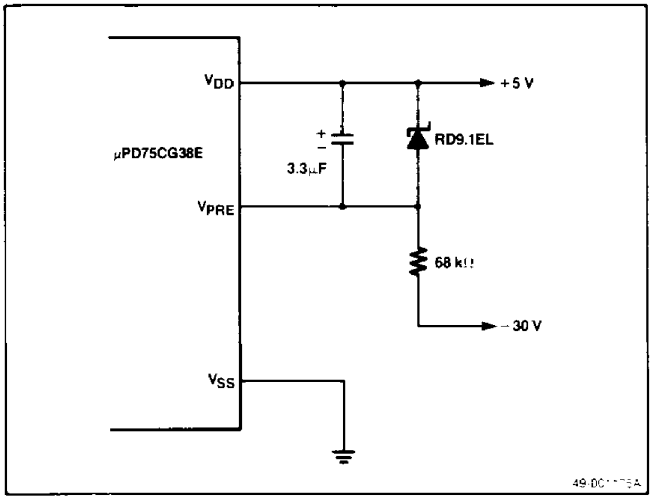
Note:

(1) $V_{PRE} = V_{DD} - 9\,V \pm 1\,V$. The circuit in figure 6 is recommended.

(2) $V_{PRE} = 0$ V

(3) Ports 4, 5, 10, 11 are output off or low input.

Figure 2. Recommended Circuit, μPD75CG38E

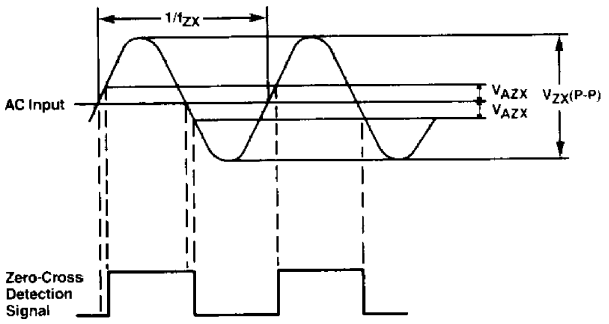


Zero-Cross Detection Characteristics

μPD7537A/38A: $T_A = -10°C$ to $+70°C$, $V_{DD} = 4.5\,V$ to $6.0\,V$
μPD75CG38E: $T_A = -10°C$ to $+70°C$, $V_{DD} = +5\,V \pm 10\%$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Zero-cross detection input voltage	$V_{ZX(P-P)}$	1.0		3.0	V_{P-P}	AC coupled, $C = 0.1\,\mu F$
Zero-cross accuracy	V_{AZX}			±100	mV	50 Hz to 60 Hz sine wave
Zero-cross detection input frequency	f_{ZX}	45		1000	Hz	

Zero-Cross Detection Waveform



Note: In the above waveforms, both 0-to-1 and 1-to-0 transitions of the zero-cross detection signal delay from the low-to-high and high-to-low transitions of the AC input signal, respectively. However, it is possible that the zero-cross detection leads low-to-high and/or high-to-low transition(s) of the AC input signal.

AC Characteristics

μPD7537A/38A

$T_A = -10°C$ to $+70°C$, $V_{DD} = +2.7\,V$ to $6.0\,V$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Cycle time (Note 1)	t_{CY}	3.3		200	μs	$V_{DD} = 4.5\,V$ to $6.0\,V$
		9.5		200	μs	
PO_0 event input frequency	f_{PO}	0		610	kHz	$V_{DD} = 4.5\,V$ to $6.0\,V$
		0		210	kHz	
PO_0 input rise time	t_{POR}			0.1	μs	
PO_0 input fall time	t_{POF}			0.1	μs	
PO_0 input pulse width, low, high	t_{POL}, t_{POH}	2.3			μs	
		0.62			μs	$V_{DD} = 4.5\,V$ to $6.0\,V$
$\overline{SCK}$ cycle time	t_{KCY}	3.0			μs	Input; $V_{DD} = 4.5\,V$ to $6.0\,V$
		3.3			μs	Output; $V_{DD} = 4.5\,V$ to $6.0\,V$
		8.0			μs	Input
		9.5			μs	Output
$\overline{SCK}$ pulse width, low	t_{KL}	4.0			μs	Input
		4.7			μs	Output
$\overline{SCK}$ pulse width, high	t_{KH}	1.3			μs	Input; $V_{DD} = 4.5\,V$ to $6.0\,V$
		1.45			μs	Output; $V_{DD} = 4.5\,V$ to $6.0\,V$
SI set-up time (to rising-edge of $\overline{SCK}$)	t_{SIK}	300			ns	
SI hold time (after rising-edge of $\overline{SCK}$)	t_{KSI}	450			ns	
SO output delay time (after falling-edge of $\overline{SCK}$)	t_{KSO}			850	ns	$V_{DD} = 4.5\,V$ to $6.0\,V$
				1200	ns	
INT0 pulse width, high, low	t_{I0H}, t_{I0L}	10			μs	
RESET pulse width, high, low	t_{RSH}, t_{RSL}	10			μs	

Note:
(1) $t_{CY} = 2/f_{CC}$ or $2/f_C$

AC Characteristics (cont)

μPD75CG38E

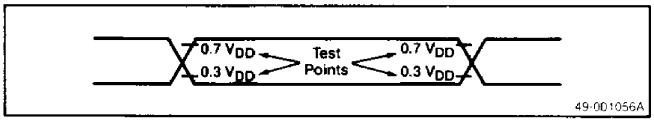
$T_A = -10°C$ to $+70°C$, $V_{DD} = +5V \pm 10\%$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Cycle time (Note 1)	t_{CY}	4.0		200	μs	
$P0_0$ event input frequency	f_{P0}	0		500	kHz	
$P0_0$ input rise time	t_{P0R}			0.2	μs	
$P0_0$ input fall time	t_{P0F}			0.2	μs	
$P0_0$ input pulse width, high, low	t_{P0H}, t_{P0L}	0.8			μs	
$\overline{SCK}$ cycle time	t_{KCY}	3.0			μs	Input
		4.0			μs	Output
$\overline{SCK}$ pulse width, low	t_{KL}	1.8			μs	Output
$\overline{SCK}$ pulse width, high	t_{KH}	1.3			μs	Input
SI set-up time (to rising-edge of $\overline{SCK}$)	t_{SIK}	300			ns	
SI hold time (after rising-edge of $\overline{SCK}$)	t_{KSI}	450			ns	
SO output delay time (after falling-edge of $\overline{SCK}$)	t_{KSO}			850	ns	
INT0 pulse width, high, low	t_{I0H}, t_{I0L}	10			μs	
RESET pulse width, high, low	t_{RSH}, t_{RSL}	10			μs	
Data input delay time from address	t_{ACC}			700	ns	
Data input delay time from $\overline{CE}$	t_{CE}			700	ns	
Input hold time after address	t_{IH}	0			ns	

Note:

(1) $t_{CY} = 2/f_{CC}$ or $2/f_C$

AC Waveform Measurement Points (Except CL1)



Oscillation Characteristics

μPD7537A/38A

$T_A = -10°C$ to $+70°C$, $V_{DD} = 2.7V$ to $6.0V$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
System clock oscillation frequency (Note 1)	f_{CC} 7537A	390	400	410	kHz	(Note 2) $V_{DD} = 4.0$ to $6.0V$
	f_{CC} 7538A	390	600	610	kHz	$V_{DD} = 4.5$ to $6.0V$
Oscillation stable time (Note 1)	t_{OS}	20			ms	(Note 3)
System clock CL1 input frequency (Note 4)	f_C	10		610	kHz	$V_{DD} = 4.5V$ to $6.0V$
		10		210	kHz	
CL1 input rise time	t_{CR}			0.1	μs	
CL1 input fall time	t_{CF}			0.1	μs	
CL1 input pulse width, low	t_{CL}	2.0		50	μs	
CL1 input pulse width, high	t_{CH}	0.7		50	μs	$V_{DD} = 4.5V$ to $6.0V$

Note:

(1) Ceramic resonator: CSB400P (MURATA) or KBR-400B (KYO-CERA) is recommended (see figure 3).

(2) Oscillation is only guaranteed at $3V \leq V_{DD} \leq 4.5V$.

(3) After V_{DD} reaches 4.5V.

(4) External clock (see figure 4).

μPD75CG38E

$T_A = -10°C$ to $+70°C$, $V_{DD} = 5V \pm 10\%$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
System clock oscillation frequency (Note 1)	f_{CC}	390	400	410	kHz	
Oscillation stable time (Note 1)	t_{OS}	20			ms	After V_{DD} reaches 4.5V
System clock CL1 input frequency (Note 2)	f_C	10		500	kHz	
CL1 input rise time	t_{CR}			0.1	μs	
CL1 input fall time	t_{CF}			0.1	μs	
CL1 input pulse width high, low	t_{CH}, t_{CL}	0.8		50	μs	

Note:

(1) Ceramic resonator: CSB400P (MURATA) is recommended; C = 300pF (see figure 3).

(2) External clock (see figure 4).

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Figure 3. Recommended Circuit, μPD7537A/7538A

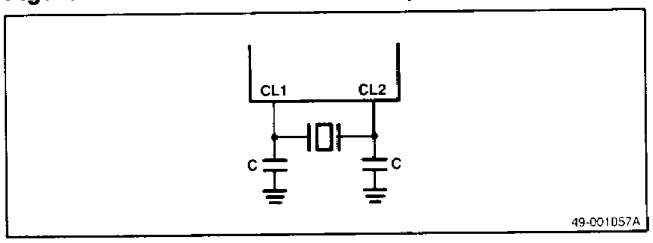
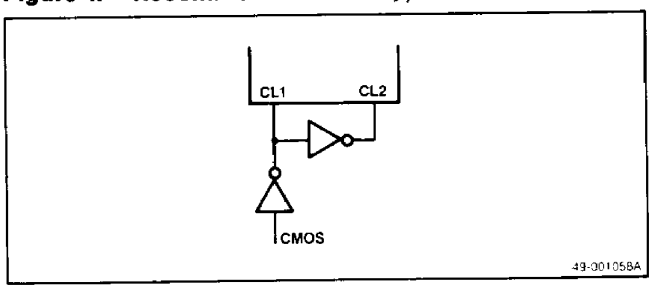


Figure 4. Recommended Circuit, μPD75CG38E



Stop Mode Low Voltage Data Retention Characteristics

μPD7537A/38A

$T_A = -10°C$ to $+70°C$, $V_{DD} = 2.7$ V to 6.0 V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Data retention supply voltage	V_{DDDR}	2.0		6.0	V	
Data retention supply current	I_{DDDR}		0.1	10	μA	$V_{DDDR} = 2$ V (Note 1)
			7	30	μA	$V_{DDDR} = 2$ V (Note 2)
RESET set-up time	t_{SRS}	0			μs	
Oscillation stable time	t_{OS}	20			ms	After V_{DD} reaches 4.5 V

μPD75CG38E

$T_A = -10°C$ to $+70°C$, $V_{DD} = 5$ V ± 10%

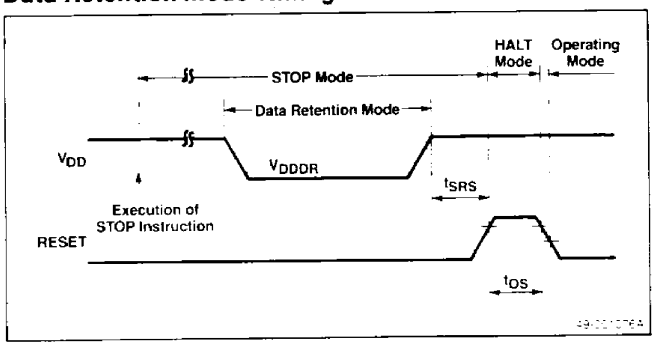
Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Data retention supply voltage	V_{DDDR}	2.0		5.5	V	
Data retention supply current	I_{DDDR}		7	30	μA	$V_{DDDR} = 2$ V
RESET set-up time	t_{SRS}	0			μs	
Oscillation stable time	t_{OS}	20			ms	After V_{DD} reaches 4.5 V

Note:

(1) Without zero-cross detector.

(2) With zero-cross detector.

Data Retention Mode Timing



μPD75CG38E EPROM Interface

A 4-Kbyte EPROM (2732) plugs into socket pins on top of the μPD75CG38E. A high input to MSEL selects the μPD7537A mode and fixes the A_{11} output high level in order to access the upper 2-Kbytes of the 4-Kbyte EPROM. When MSEL is open, μPD7538A mode is selected. All EPROM addresses can be accessed because A_{11} functions as the MSB of the address. Figure 5 shows the address control unit. Figures 6 and 7 show the μPD75CG38E connected with the 2732.

Figure 8 shows the EPROM read timing. Data is read into the instruction buffer at the end of the T4 state. The chip enable ($\overline{CE}$) signal is made active during 2 states (T3, T4) in order to decrease the power consumption of the EPROM.

Figure 5. Address Control Unit

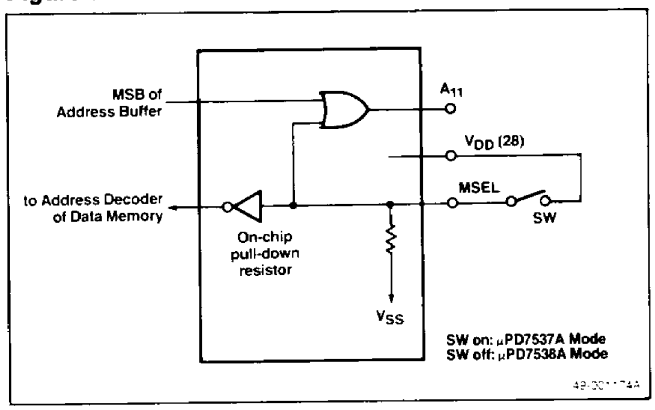


Figure 6. Connection with the 2732 (μPD7537A Mode)

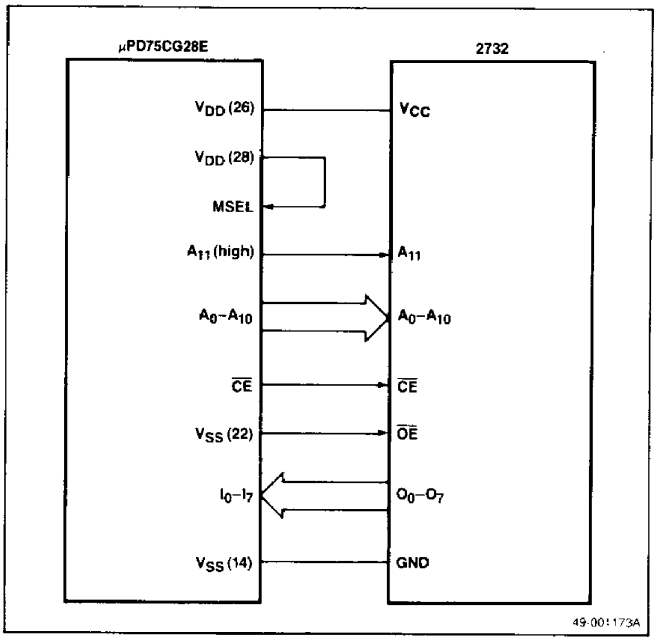


Figure 7. Connection with the 2732 (μPD7538A Mode)

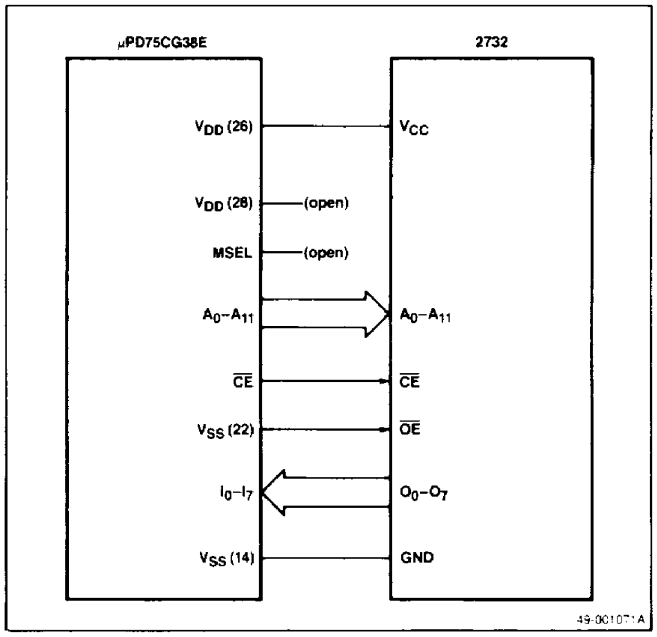
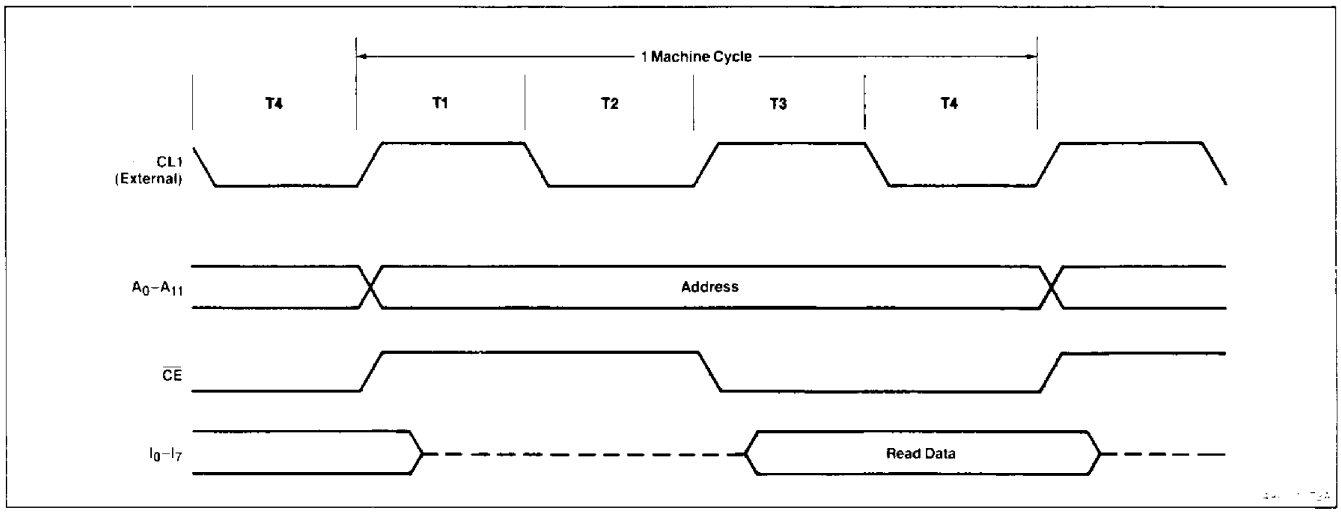


Figure 8. EPROM Read Timing



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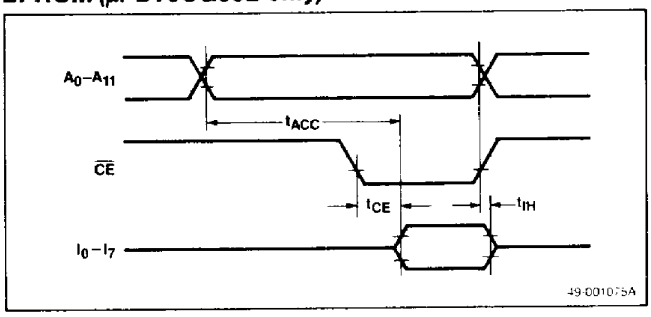
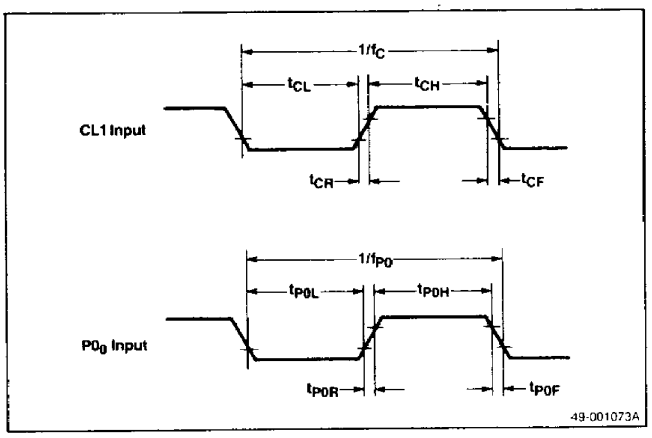
Timing Waveforms

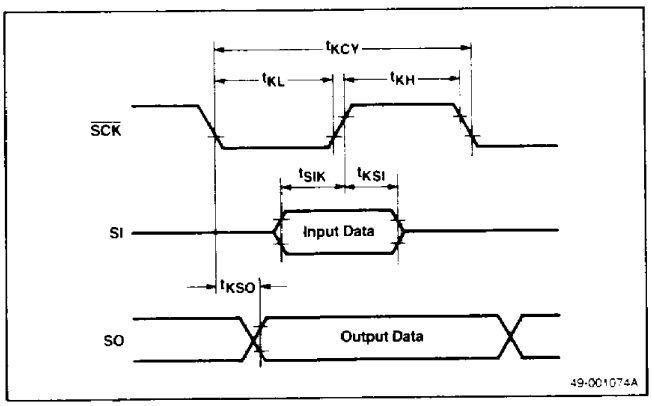
EPROM (μPD75CG38E only)



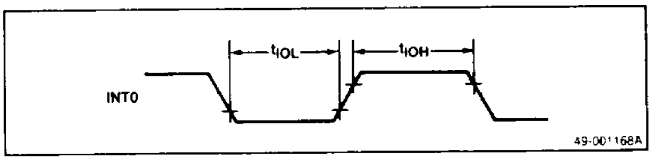
Clock



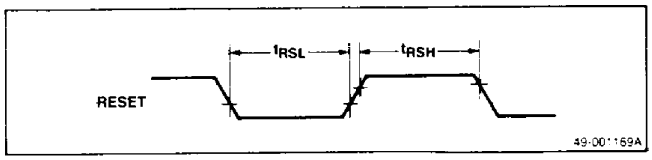
Serial Interface



Interrupt Input



Reset Input



Differences Among the μPD7537A/38A/CG38E

	μPD75CG38E	μPD7537A	μPD7538A
Program memory	4 Kbyte EPROM (2732) connectable on top	On-chip 2 Kbyte ROM	On-chip 4 Kbyte ROM
Data memory (RAM)	160×4	128×4	160×4
High-voltage output lines	All open-drain outputs	On-chip load resistor or open drain output (bit by bit, mask optional)	
V_{LOAD} pin	No	Yes	
Zero-cross detection	Yes	Mask optional	
Package	42-pin ceramic piggyback DIP bottom pin compatible with μPD7537A / 38A	42-pin plastic DIP 42-pin plastic shrink DIP	
Power supply	5 V	2.7 V to 6.0 V	

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