

### Description

The μPD7502 and μPD7503 4-bit, single-chip CMOS microcomputers have advanced fourth-generation architecture with the functional blocks necessary for a single-chip controller, including an 8-bit timer/event counter, an 8-bit serial I/O, and an LCD controller/driver.

The instruction set includes the following types of instructions: addressing, table look-up, bit manipulation, vectored jump, auto increment or decrement data pointer, and conditional skip. These instructions maximize use of fixed program memory space.

Both devices are manufactured with the CMOS process and have a maximum power consumption of 900 μA at 5 V and 300 μA at 3 V. Halt and stop modes further reduce power consumption.

These devices are ideal for a wide range of solar- and battery-powered applications.

### Features

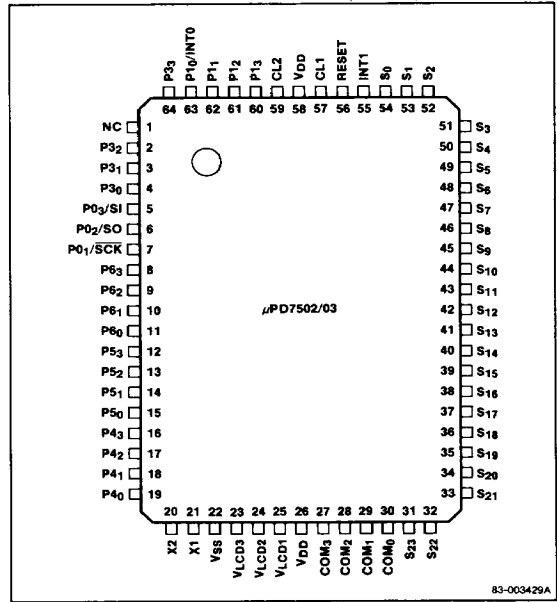
- 92 powerful instructions
- Program ROM
  - μPD7502: 2048 x 8-bit
  - μPD7503: 4096 x 8-bit
- Data RAM
  - μPD7502: 128 x 4-bit
  - μPD7503: 224 x 4-bit
- Interrupts
  - External: INT0, INT1
  - Internal: INTT (timer/event counter)
  - INTS (serial interface)
- 8-bit timer/event counter
  - Based on crystal oscillation
  - External event counter (prescale option by 64)
- Serial interface
- LCD controller/driver
  - Programmable multiplexing mode: triplex, quadruplex, or pseudo-static
  - 4 common lines (COM<sub>0</sub>-COM<sub>3</sub>)
  - 24 segment lines (S<sub>0</sub>-S<sub>23</sub>)
- Standby modes: stop, halt
- Data retention mode
- I/O ports
  - 3-bit input port
  - 4-bit input port
  - 4-bit output port
  - Two 4-bit I/O ports with 8-bit capability
  - 4-bit I/O port with each bit configurable as an input or output

- RC oscillation clock
- Crystal oscillation clock
- 2.5 to 6.0 V operating voltage
- CMOS technology

### Ordering Information

Part No.	Package Type	Max Frequency of Operation
μPD7502GF-12	64-pin plastic QFP	410 kHz
μPD7503GF-12	64-pin plastic QFP	410 kHz

### Pin Configuration



3

**Pin Identification**

No.	Symbol	Function
1	NC	No connection
2-4, 64	P3 <sub>3</sub> -P3 <sub>0</sub>	4-bit output port 3
5-7	P0 <sub>3</sub> /SI P0 <sub>2</sub> /SO P0 <sub>1</sub> /SCK	3-bit input port 0, or serial I/O interface
8-11	P6 <sub>3</sub> -P6 <sub>0</sub>	4-bit I/O port 6
12-15	P5 <sub>3</sub> -P5 <sub>0</sub>	4-bit I/O port 5
16-19	P4 <sub>3</sub> -P4 <sub>0</sub>	4-bit I/O port 4
20, 21	X2, X1	Crystal clock/external event input port X
22	V <sub>SS</sub>	Ground
23-25	V <sub>LCD3</sub> -V <sub>LCD1</sub>	LCD bias supply inputs
26, 58	V <sub>DD</sub>	Positive power supply
27-30	COM <sub>3</sub> -COM <sub>0</sub>	LCD backplane driver outputs
31-54	S <sub>23</sub> -S <sub>0</sub>	LCD segment driver outputs
55	INT1	External interrupt
56	RESET	RESET input
57, 59	CL1, CL2	System clock input
60-63	P1 <sub>3</sub> -P1 <sub>1</sub> , P1 <sub>0</sub> /INT0	4-bit input port 1, or external interrupt INT0

**Status of Unused Pins**

Name	Pin Connection
CL2	Open
X1	V <sub>SS</sub>
X2	Open
P0 <sub>1</sub> /SCK P0 <sub>2</sub> /SO P0 <sub>3</sub> /SI	V <sub>SS</sub> or V <sub>DD</sub>
P1 <sub>0</sub> /INT0	V <sub>SS</sub>
P1 <sub>1</sub> -P1 <sub>3</sub>	V <sub>SS</sub> or V <sub>DD</sub>
P3 <sub>0</sub> -P3 <sub>3</sub>	Open
P4 <sub>0</sub> -P4 <sub>3</sub> P5 <sub>0</sub> -P5 <sub>3</sub> P6 <sub>0</sub> -P6 <sub>3</sub>	Input mode: V <sub>SS</sub> or V <sub>DD</sub> Output mode: Open
INT1	V <sub>SS</sub>
S <sub>0</sub> -S <sub>23</sub> COM <sub>0</sub> -COM <sub>3</sub> V <sub>LCD1</sub> -V <sub>LCD3</sub>	Open

## Pin Functions

### P0<sub>3</sub>/SI, P0<sub>2</sub>/SO, P0<sub>1</sub>/SCK [Port 0 or Serial Interface]

This port can be configured as a 4-bit parallel input port 0 or as the 8-bit serial I/O interface under control of the serial mode select register. The serial interface consists of the serial input (SI), the serial output (SO), and the serial clock (SCK), which synchronizes data transfer.

### P1<sub>3</sub>-P1<sub>1</sub>, P1<sub>0</sub>/INT0 [Port 1 or Interrupt]

4-bit input port 1. Line P1<sub>0</sub> is shared with external interrupt INT0, which is a rising edge-triggered interrupt.

### P3<sub>3</sub>-P3<sub>0</sub> [Port 3]

4-bit, latched three-state output port 3.

### P4<sub>3</sub>-P4<sub>0</sub> [Port 4]

4-bit input or latched three-state output port 4. Can perform 8-bit I/O in conjunction with port 5.

### P5<sub>3</sub>-P5<sub>0</sub> [Port 5]

4-bit input or latched three-state output port 5. Can perform 8-bit I/O in conjunction with port 4.

### P6<sub>3</sub>-P6<sub>0</sub> [Port 6]

4-bit input or latched three-state output port 6. The port 6 mode select register configures individual lines as inputs or outputs.

### COM<sub>3</sub>-COM<sub>0</sub> [LCD Backplane Driver Outputs]

LCD backplane driver outputs.

### S<sub>23</sub>-S<sub>0</sub> [LCD Segment Driver Outputs]

LCD segment driver outputs.

### INT1 [Interrupt]

This external interrupt is a rising edge-triggered interrupt latched by CL.

### RESET

A high-level input to this pin initializes the μPD7502/7503.

### X2, X1 [Crystal Clock/External Event Input Port X]

For crystal clock operation, connect a crystal oscillator circuit to input X1 and output X2. For external event counting, input external event pulses to X1 and leave X2 open.

### CL1, CL2 [System Clock Input]

Connect an 82-kΩ resistor across CL1 and CL2, and a 33-pF capacitor from CL1 to V<sub>SS</sub>. Or, connect an external clock source to CL1 and leave CL2 open.

### V<sub>LCD3</sub>-V<sub>LCD1</sub> [LCD Bias Voltage Inputs]

LCD bias voltage supply inputs to the LCD voltage controller. Apply appropriate voltages from a voltage ladder connected across V<sub>DD</sub>.

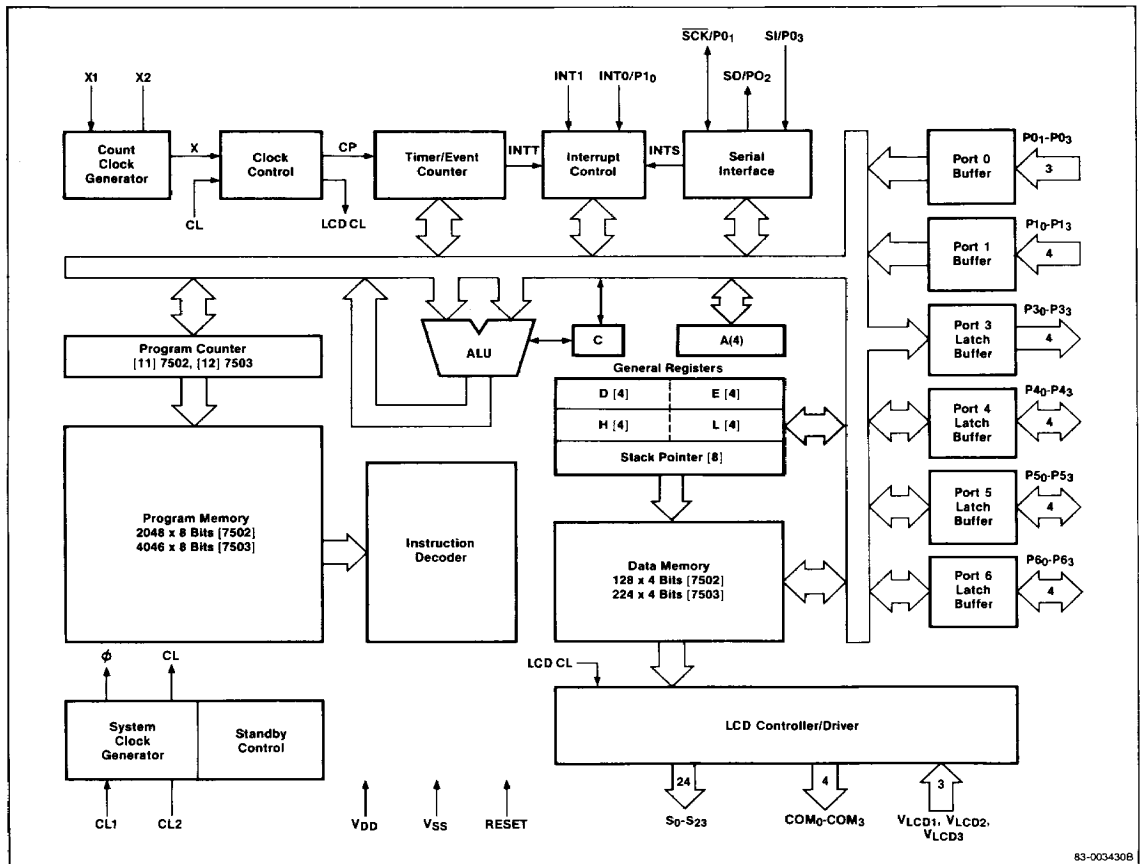
### V<sub>DD</sub>

Positive power supply. For proper operation, apply a single voltage from 2.5 to 6.0 V.

### V<sub>SS</sub>

Ground.

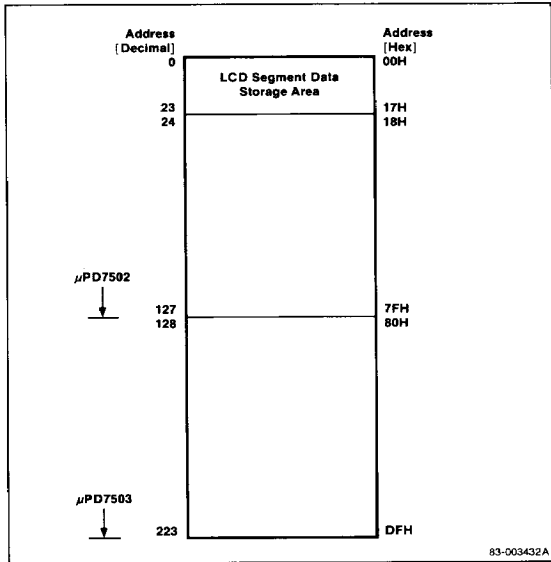
**Block Diagram**



See figures 1 through 8 for additional block diagram details.

Figure	Title
1	Data Memory Map
2	Program Memory Map
3	Interface at Input/Output Ports
4	Clock Control
5	Timer/Event Counter
6	Interrupt Control
7	Serial Interface
8	LCD Controller/Driver

**Figure 1. Data Memory Map**



**Figure 2. Program Memory Map**

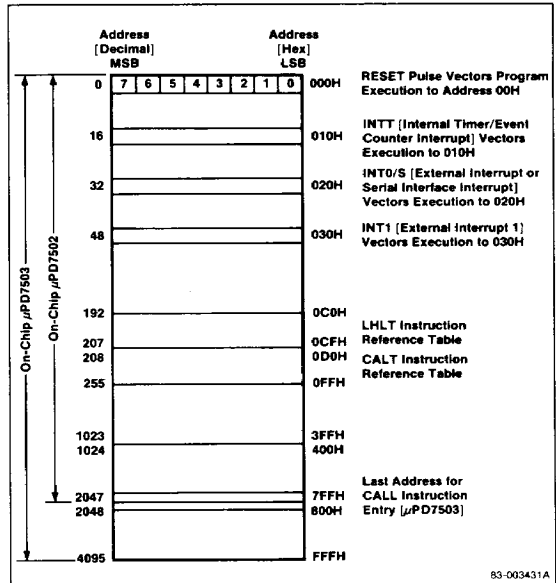
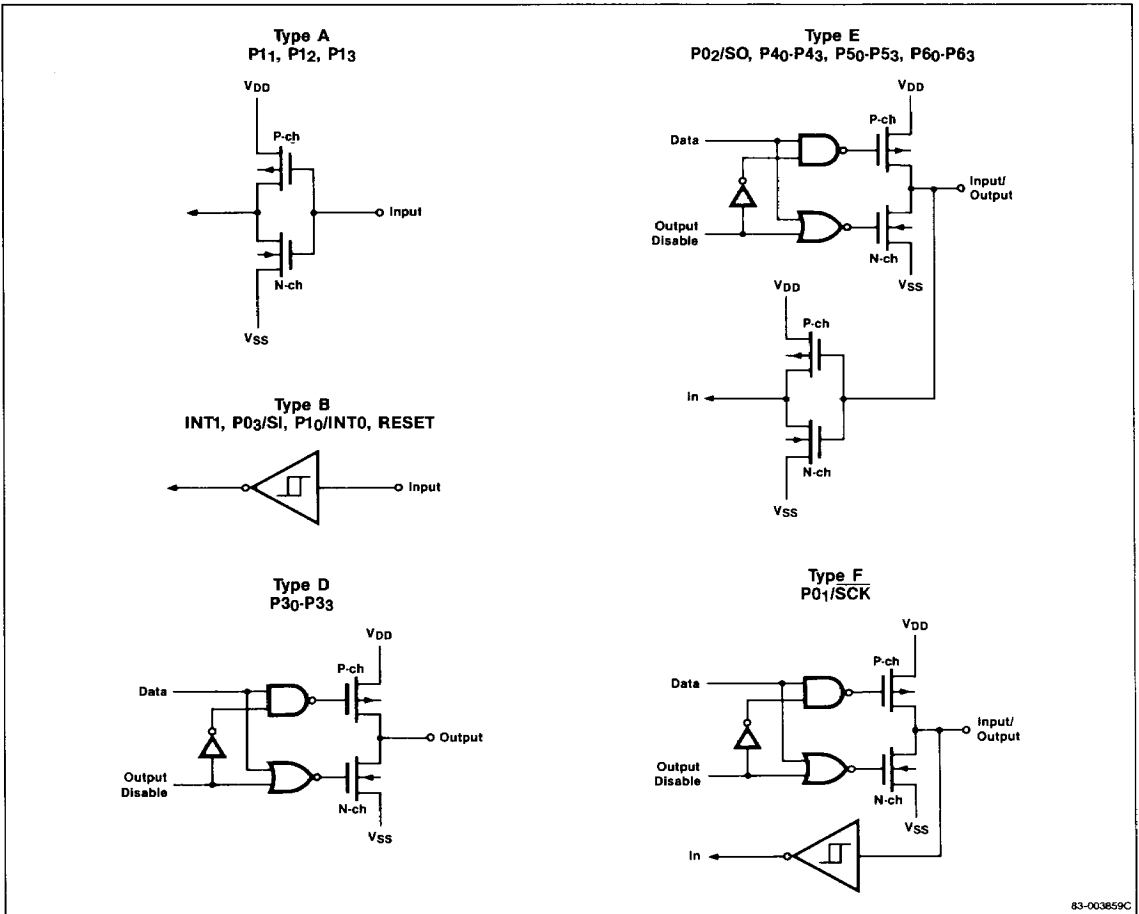
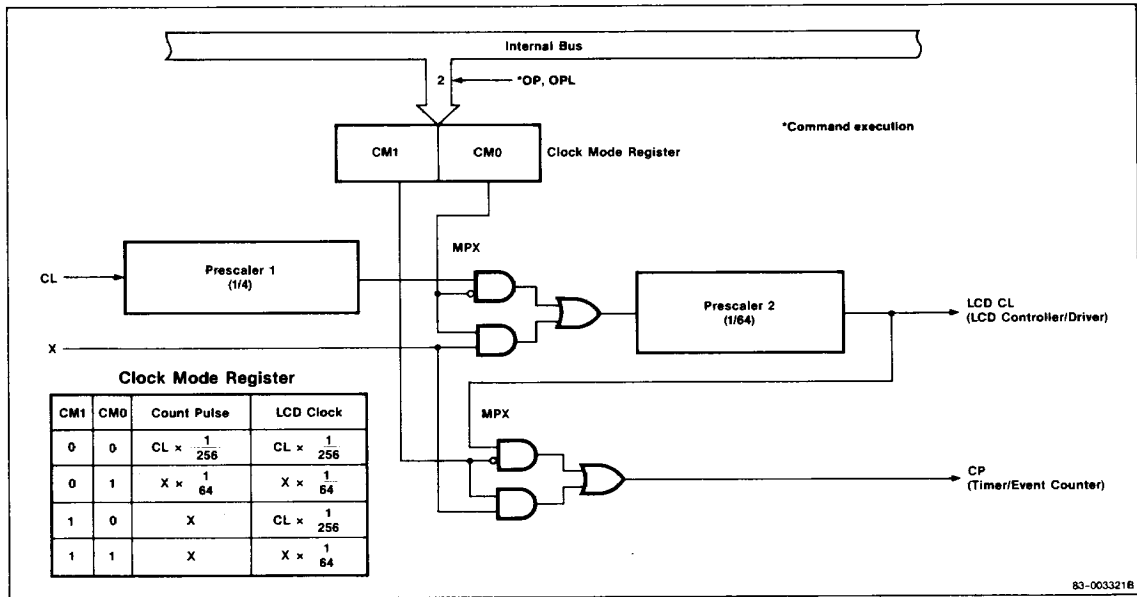


Figure 3. Interface at Input/Output Ports



63-003859C

**Figure 4. Clock Control**



3

**Figure 5. Timer/Event Counter**

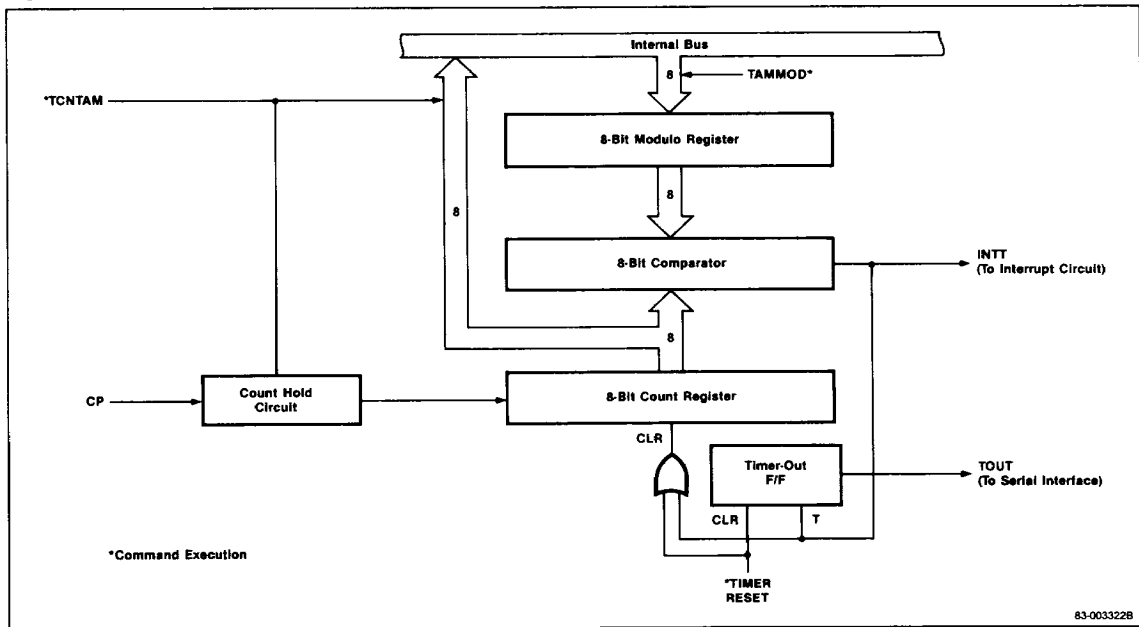
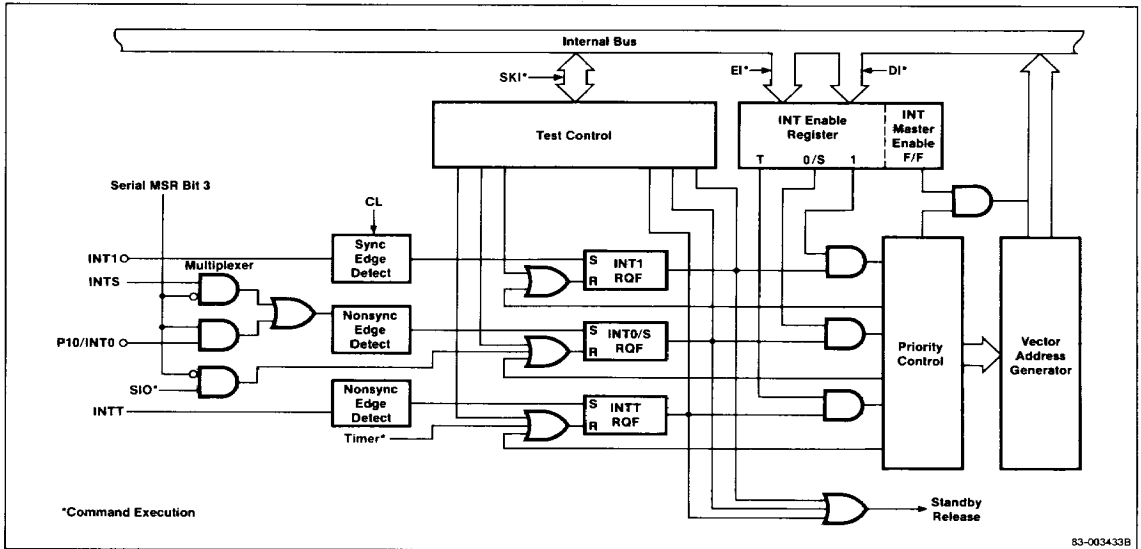
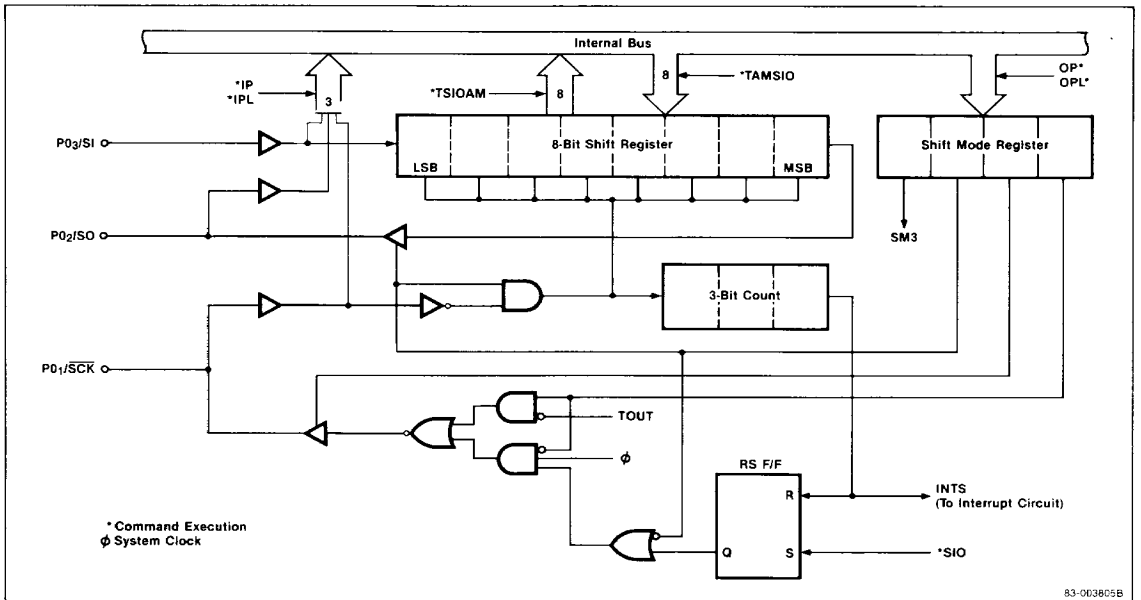


Figure 6. Interrupt Control



83-003433B

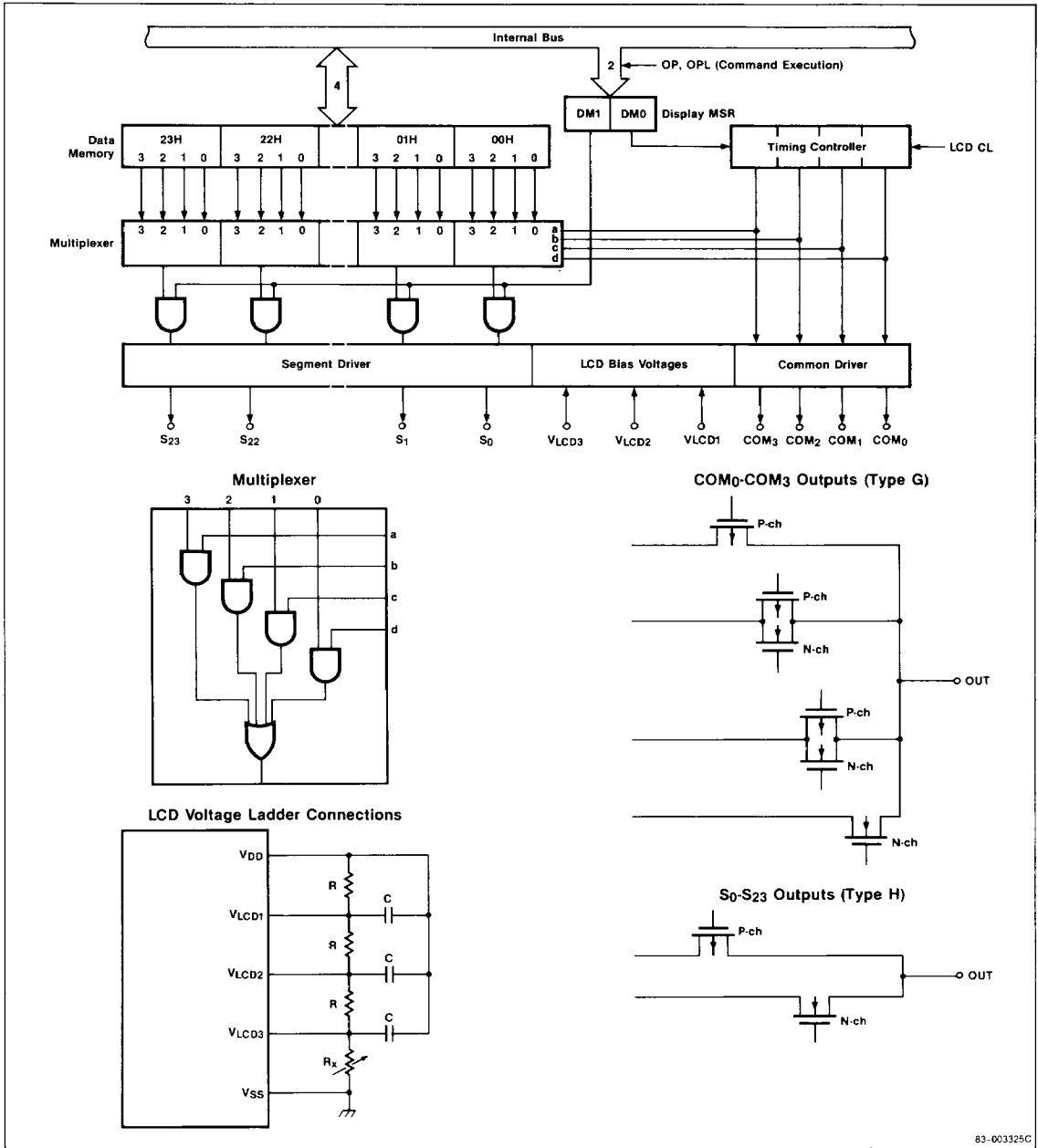
Figure 7. Serial Interface



83-003805B



Figure 8. LCD Controller/Driver



3

83-003325C

**Absolute Maximum Ratings**

T<sub>A</sub> = 25°C

Power supply voltage, V <sub>DD</sub>	-0.3 to +7.0 V
All input and output voltages	-0.3 V to V <sub>DD</sub> + 0.3 V
Output current high, I <sub>OH</sub>	
Per pin	-17 mA
Total, output ports	-20 mA
Output current low, I <sub>OL</sub>	
Per pin	17 mA
Total, output ports	55 mA
Operating temperature, T <sub>OPT</sub>	-10 to +70°C
Storage temperature, T <sub>STG</sub>	-65 to +150°C

**Capacitance**

T<sub>A</sub> = 25°C; V<sub>DD</sub> = 0 V

Parameter	Symbol	Limits			Unit	Test Conditions
		Min	Typ	Max		
Input capacitance	C <sub>I</sub>		15		pF	f <sub>C</sub> = 1 MHz Unmeasured pins returned to V <sub>SS</sub>
Output capacitance	C <sub>O</sub>		15		pF	
I/O capacitance	C <sub>IO</sub>		15		pF	

**Comment:** Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**DC Characteristics 1**

For V<sub>DD</sub> = 2.5 to 3.3 Volts

T<sub>A</sub> = -10 to +70°C

Parameter	Symbol	Limits			Unit	Test Conditions
		Min	Typ	Max		
Input voltage, high	V <sub>IH1</sub>	0.8 V <sub>DD</sub>		V <sub>DD</sub>	V	Except CL1, X1
	V <sub>IH2</sub>	V <sub>DD</sub> - 0.3		V <sub>DD</sub>	V	CL1, X1
	V <sub>IHDR</sub>	0.9 V <sub>DDDR</sub>		V <sub>DDDR</sub> + 0.2	V	RESET, data retention mode
Input voltage, low	V <sub>IL1</sub>	0		0.2 V <sub>DD</sub>	V	Except CL1, X1
	V <sub>IL2</sub>	0		0.3	V	CL1, X1
Output voltage, high	V <sub>OH</sub>	V <sub>DD</sub> - 0.5			V	I <sub>OH</sub> = -80 μA
Output voltage, low	V <sub>OL</sub>			0.5	V	I <sub>OL</sub> = 350 μA
Input leakage current, high	I <sub>LIH1</sub>			3	μA	Except CL1, X1; V <sub>IN</sub> = V <sub>DD</sub>
	I <sub>LIH2</sub>			10	μA	CL1, X1; V <sub>IN</sub> = V <sub>DD</sub>
Input leakage current, low	I <sub>LIL1</sub>			-3	μA	Except CL1, X1; V <sub>IN</sub> = 0 V
	I <sub>LIL2</sub>			-10	μA	CL1, X1; V <sub>IN</sub> = 0 V
Output leakage current, high	I <sub>LOH</sub>			3	μA	V <sub>O</sub> = V <sub>DD</sub>
Output leakage current, low	I <sub>LOL</sub>			-3	μA	V <sub>O</sub> = 0 V
Supply voltage	V <sub>DDDR</sub>	2.0			V	Data retention mode
Supply current	I <sub>DD1</sub>		50	250	μA	Normal operation, V <sub>DD</sub> = 3 V ± 10%; R = 240 kΩ ± 2%, C = 33 pF ± 5%
			35	230	μA	Normal operation, V <sub>DD</sub> = 2.5 V; R = 240 kΩ ± 2%, C = 33 pF ± 5%
	I <sub>DD2</sub>		0.3	10	μA	Stop mode, X1 = 0 V; V <sub>DD</sub> = 3 V ± 10%
			0.2	10	μA	Stop mode, X1 = 0 V; V <sub>DD</sub> = 2.5 V
I <sub>DDDR</sub>		0.2	10	μA	Data retention mode, V <sub>DDDR</sub> = 2.0 V	

## DC Characteristics 2

For  $V_{DD} = 2.7$  to  $6.0$  Volts

$T_A = -10$  to  $+70^\circ\text{C}$

Parameter	Symbol	Limits			Unit	Test Conditions
		Min	Typ	Max		
Input voltage, high	$V_{IH1}$	$0.7 V_{DD}$		$V_{DD}$	V	Except CL1, X1
	$V_{IH2}$	$V_{DD} - 0.5$		$V_{DD}$	V	CL1, X1
	$V_{IHDR}$	$0.9 V_{DDDR}$		$V_{DDDR} + 0.2$		RESET, data retention mode
Input voltage, low	$V_{IL1}$	0		$0.3 V_{DD}$	V	Except CL1, X1
	$V_{IL2}$	0		0.5	V	CL1, X1
Output voltage, high	$V_{OH}$	$V_{DD} - 1.0$			V	$I_{OH} = -1.0$ mA, $V_{DD} = 4.5$ to $6.0$ V
		$V_{DD} - 0.5$			V	$I_{OL} = -100$ μA
Output voltage, low	$V_{OL}$			0.4	V	$I_{OL} = 1.6$ mA, $V_{DD} = 4.5$ to $6.0$ V
				0.5	V	$I_{OL} = 400$ μA
Input leakage current, high	$I_{LIH1}$			3	μA	Except CL1, X1; $V_I = V_{DD}$
	$I_{LIH2}$			10	μA	CL1, X1
Input leakage current, low	$I_{LIL1}$			-3	μA	Except CL1, X1; $V_I = 0$ V
	$I_{LIL2}$			-10	μA	CL1, X1
Output leakage current, high	$I_{LOH}$			3	μA	$V_O = V_{DD}$
Output leakage current, low	$I_{LOL}$			-3	μA	$V_O = 0$ V
Output impedance (1)	$R_{COM}$		3	5	kΩ	COM <sub>0</sub> -COM <sub>3</sub> ; $V_{DD} = 4.5$ to $6.0$ V
			5	15	kΩ	COM <sub>0</sub> -COM <sub>3</sub>
			15	20	kΩ	S <sub>0</sub> -S <sub>23</sub> ; $V_{DD} = 4.5$ to $6.0$ V
		20	60	kΩ	S <sub>0</sub> -S <sub>23</sub>	
Supply voltage	$V_{DDDR}$	2.0		6.0	V	Data retention mode
Supply current	$I_{DD1}$		300	900	μA	Normal operation, $V_{DD} = 5$ V $\pm$ 10%; R = 82 kΩ $\pm$ 2%, C = 33 pF $\pm$ 5%
			70	300	μA	Normal operation, $V_{DD} = 3$ V $\pm$ 10%; R = 160 kΩ $\pm$ 2%, C = 33 pF $\pm$ 5%
	$I_{DD2}$		1.0	20	μA	Stop mode, X1 = 0 V; $V_{DD} = 5$ V $\pm$ 10%
			0.3	10	μA	Stop mode, X1 = 0 V; $V_{DD} = 3$ V $\pm$ 10%
	$I_{DDDR}$		0.2	10	μA	Data retention mode, $V_{DDDR} = 2.0$ V

**Note:**

- (1)  $V_{LCD} = 2.7$  V to  $V_{DD}$
- $V_{LCD1} = V_{DD} - (1/3) V_{LCD}$
- $V_{LCD2} = V_{DD} - (2/3) V_{LCD}$
- $V_{LCD3} = V_{DD} - V_{LCD}$

3

**AC Characteristics 1**

For  $V_{DD} = 2.7$  to  $6.0$  Volts

$T_A = -10$  to  $+70$  °C

Parameter	Symbol	Limits			Unit	Test Conditions		
		Min	Typ	Max				
System clock frequency	$f_{CC}$	150	200	240	kHz	$V_{DD} = 5\text{ V} \pm 10\%$ ; $R = 82\text{ k}\Omega \pm 2\%$ (Note 1)		
		75	100	120			kHz	$V_{DD} = 3\text{ V} \pm 10\%$ ; $R = 160\text{ k}\Omega \pm 2\%$ (Note 1)
		75		135				
	$f_C$	10		410	kHz	CL1, external clock, 50% duty; $V_{DD} = 4.5$ to $6.0\text{ V}$		
	10		125	kHz			CL1, external clock, 50% duty; $V_{DD} = 2.7\text{ V}$	
System clock rise and fall time	$t_{CR}, t_{CF}$			0.2	$\mu\text{s}$	CL1, external clock		
System clock pulse width	$t_{CH}, t_{CL}$	1.2		50	$\mu\text{s}$	CL1, external clock; $V_{DD} = 4.5$ to $6.0\text{ V}$		
		4.0		50	$\mu\text{s}$	CL1, external clock; $V_{DD} = 2.7\text{ V}$		
Counter clock frequency	$f_{XX}$	25	32	50	kHz	X1, X2, crystal oscillator		
	$f_X$	0		410	kHz	X1, external pulse input, 50% duty; $V_{DD} = 4.5$ to $6.0\text{ V}$		
		0		125			kHz	X1, external pulse input, 50% duty; $V_{DD} = 2.7\text{ V}$
Counter clock rise and fall time	$t_{XR}, t_{XF}$			0.2	$\mu\text{s}$	X1, external pulse input		
Counter clock pulse width	$t_{XH}, t_{XL}$	1.2			$\mu\text{s}$	X1, external pulse input; $V_{DD} = 4.5$ to $6.0\text{ V}$		
		4.0			$\mu\text{s}$	X1, external pulse input; $V_{DD} = 2.7\text{ V}$		
SCK cycle time	$t_{KCY}$	3.0			$\mu\text{s}$	$\overline{\text{SCK}}$ as input; $V_{DD} = 4.5$ to $6.0\text{ V}$		
		8.0			$\mu\text{s}$	$\overline{\text{SCK}}$ as input		
		4.9			$\mu\text{s}$	$\overline{\text{SCK}}$ as output; $V_{DD} = 4.5$ to $6.0\text{ V}$		
		16.0			$\mu\text{s}$	$\overline{\text{SCK}}$ as output		
SCK pulse width	$t_{KH}, t_{KL}$	1.3			$\mu\text{s}$	$\overline{\text{SCK}}$ as input; $V_{DD} = 4.5$ to $6.0\text{ V}$		
		4.0			$\mu\text{s}$	$\overline{\text{SCK}}$ as input		
		2.2			$\mu\text{s}$	$\overline{\text{SCK}}$ as output; $V_{DD} = 4.5$ to $6.0\text{ V}$		
		8.0			$\mu\text{s}$	$\overline{\text{SCK}}$ as output		
SI setup time to $\overline{\text{SCK}} \uparrow$	$t_{SIK}$	300			ns			
SI hold time after $\overline{\text{SCK}} \uparrow$	$t_{KSI}$	450			ns			
SO delay time after $\overline{\text{SCK}} \downarrow$	$t_{KSO}$			850	ns	$V_{DD} = 4.5\text{ V}$ to $6.0\text{ V}$		
				1200	ns			
INT0 pulse width	$t_{I0H}, t_{I0L}$	10			$\mu\text{s}$			
INT1 pulse width	$t_{I1H}, t_{I1L}$	(Note 2)			$\mu\text{s}$			
RESET pulse width	$t_{RSH}, t_{RSL}$	10			$\mu\text{s}$			
RESET setup time	$t_{SRS}$	0			ns			
RESET hold time	$t_{HRS}$	0			ns			

**Notes:**

(1) RC network at CL1 and CL2;  $C = 33\text{ pF} \pm 5\%$ ,  $|\Delta C / ^\circ\text{C}| \leq 60\text{ ppm}$ .

(2)  $2 \times 10^3 \div f_{cc}$  or  $f_c$  in kHz.

## AC Characteristics 2

For  $V_{DD} = 2.5$  to  $3.3$  Volts

$T_A = -10$  to  $+70^\circ\text{C}$

Parameter	Symbol	Limits			Unit	Test Conditions
		Min	Typ	Max		
System clock frequency	$f_{CC}$	50		80	kHz	$R = 240\text{ k}\Omega \pm 2\%$ (Note 1)
		50	64	77		$V_{DD} = 2.5\text{ V}; R = 240\text{ k}\Omega \pm 2\%$ (Note 1)
	$f_C$	10		80	kHz	CL1, external clock, 50% duty
System clock rise and fall time	$t_{CR}, t_{CF}$			0.2	$\mu\text{s}$	CL1, external clock
System clock pulse width	$t_{CH}, t_{CL}$	6.25		50	$\mu\text{s}$	CL1, external clock
Counter clock frequency	$f_{XX}$	25	32	50	kHz	X1, X2, crystal oscillator
	$f_X$	0		80	kHz	X1, external pulse input, 50% duty
Counter clock rise and fall time	$t_{XR}, t_{XF}$			0.2	$\mu\text{s}$	X1, external pulse input
Counter clock pulse width	$t_{XH}, t_{XL}$	6.25			$\mu\text{s}$	X1, external pulse input
$\overline{\text{SCK}}$ cycle time	$t_{KCY}$	12.5			$\mu\text{s}$	$\overline{\text{SCK}}$ as input
		25			$\mu\text{s}$	$\overline{\text{SCK}}$ as output
$\overline{\text{SCK}}$ pulse width	$t_{KH}, t_{KL}$	6.25			$\mu\text{s}$	$\overline{\text{SCK}}$ as input
		11.5			$\mu\text{s}$	$\overline{\text{SCK}}$ as output
SI setup time to $\overline{\text{SCK}} \uparrow$	$t_{SIK}$	1			$\mu\text{s}$	
SI hold time after $\overline{\text{SCK}} \uparrow$	$t_{KSI}$	1			$\mu\text{s}$	
SO delay time after $\overline{\text{SCK}} \downarrow$	$t_{KSO}$			2	$\mu\text{s}$	
INT0 pulse width	$t_{0H}, t_{0L}$	30			$\mu\text{s}$	
INT1 pulse width	$t_{1H}, t_{1L}$	(Note 2)			$\mu\text{s}$	
RESET pulse width	$t_{RSH}, t_{RSL}$	30			$\mu\text{s}$	

### Notes:

(1) RC network at CL1 and CL2;  $C = 33\text{ pF} \pm 5\%$ ,  $|\Delta C/^\circ\text{C}| \leq 60\text{ ppm}$ .

(2)  $2 \times 10^3 \div f_{CC}$  or  $f_C$  in kHz.

## Recommended R and C Values for System Clock Oscillation Circuit

$T_A = -10$  to  $+70^\circ\text{C}$

Supply Voltage Range	Recommended Values (Note 1)	Frequency Range
4.5 to 6.0 V	$R = 82\text{ k}\Omega \pm 2\%$	150 to 250 kHz, 200 kHz typical
2.7 to 3.3 V	$R = 160\text{ k}\Omega \pm 2\%$	75 to 120 kHz, 100 kHz typical
2.7 to 6.0 V	$R = 160\text{ k}\Omega \pm 2\%$	75 to 135 kHz
2.5 to 3.3 V	$R = 240\text{ k}\Omega \pm 2\%$	50 to 80 kHz
2.5 to 6.0 V	$R = 240\text{ k}\Omega \pm 2\%$	50 to 85 kHz

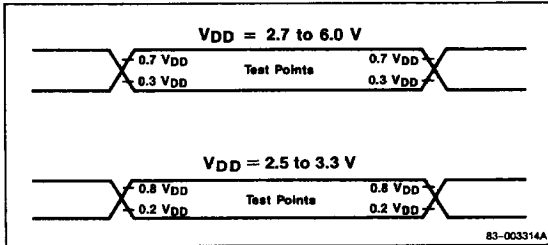
### Note:

(1)  $C = 33\text{ pF} \pm 5\%$ ,  $|\Delta C/^\circ\text{C}| \leq 60\text{ ppm}$ .

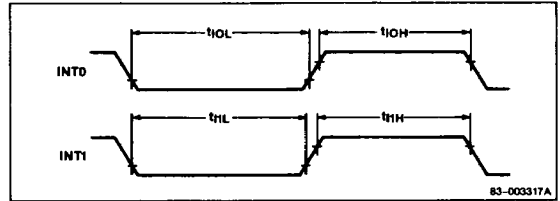
3

## Timing Waveforms

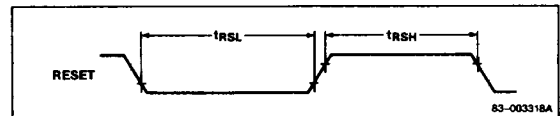
### Timing Measurement Points



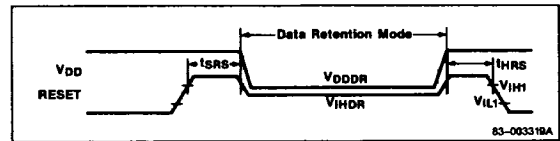
### External Interrupts



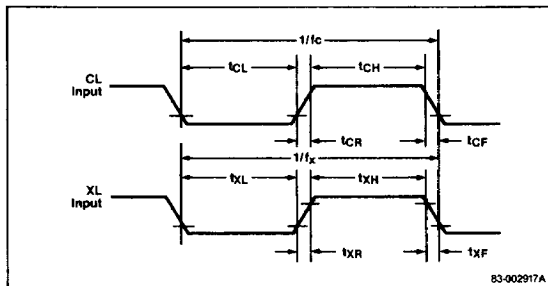
### Reset



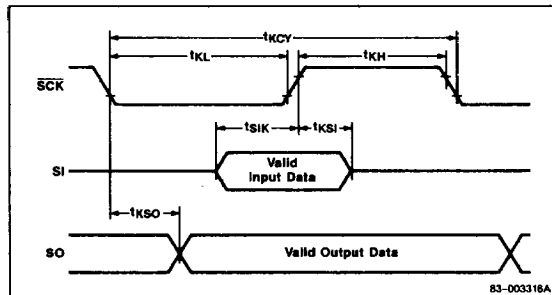
### Data Retention Mode



### Clock Timing



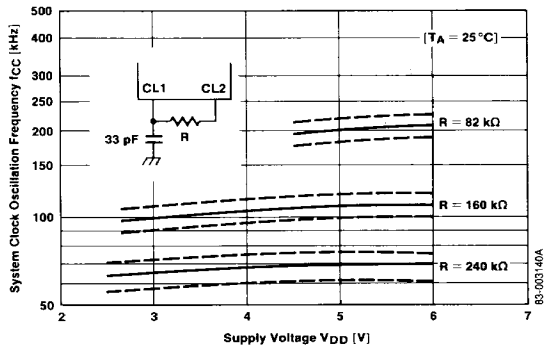
### Serial Interface



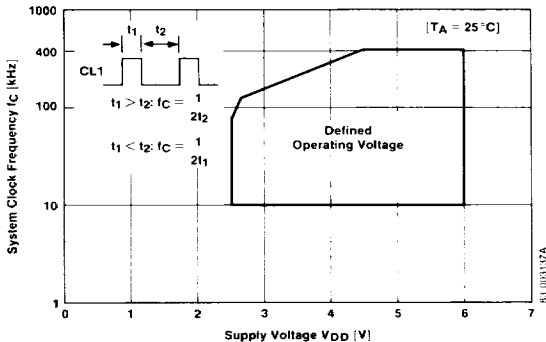
## Operating Characteristics

T<sub>A</sub> = 25°C

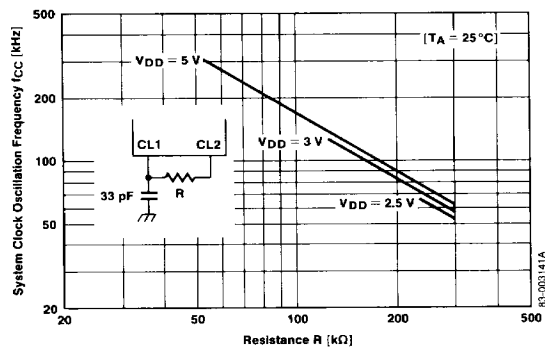
f<sub>CC</sub> vs V<sub>DD</sub>



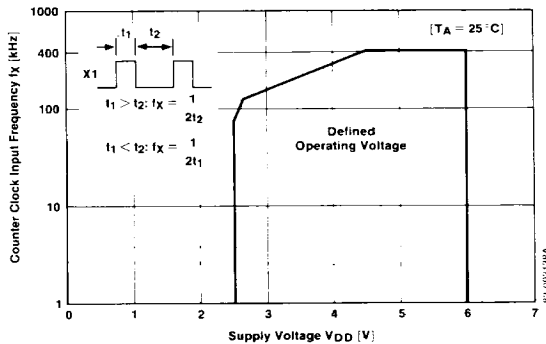
f<sub>C</sub> vs V<sub>DD</sub> [External Clock]



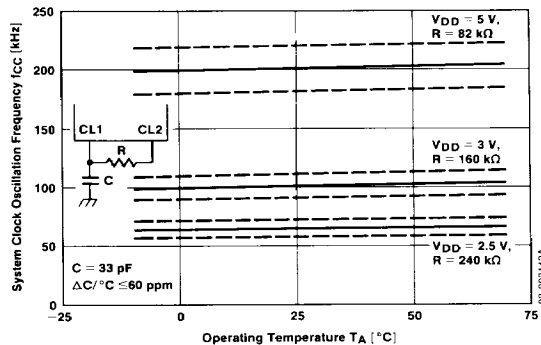
f<sub>CC</sub> vs R



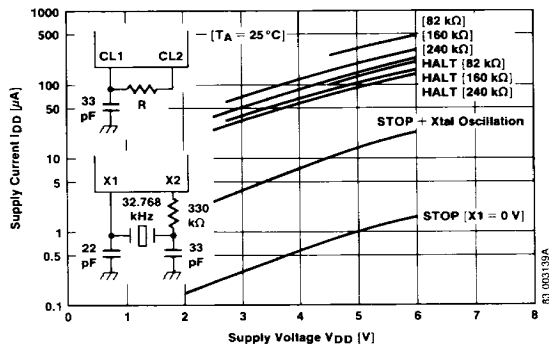
f<sub>X</sub> vs V<sub>DD</sub> [External Clock]



f<sub>CC</sub> vs T<sub>A</sub>



I<sub>DD</sub> vs V<sub>DD</sub>



Operating Characteristics (cont)

