TYPES 3N204, 3N205, 3N206
N-CHANNEL DUAL-GATE DEPLETION-TYPE INSULATED-GATE FIELD-EFFECT TRANSISTORS

BULLETIN NO. DL-S 7211717, MAY 1972

DEPLETION-TYPE MOS SILICON TRANSISTORS

- Monolithic Gate-Protection Diodes
- Low C_{rss} . . . 0.03 pF Max
- High $|y_{fs}|$ . . . 14,000 μmhos Typ

description

The 3N204, 3N205, and 3N206 are N-channel, depletion-type, dual-gate, metal-oxide-semiconductor transistors. They are protected from excessive input voltages by integrated back-to-back diodes between gates and source, thus eliminating precautionary handling procedures required by unprotected MOS transistors. These transistors are ideally suited for many applications which previously only vacuum tubes could fulfill.

The 3N204 is intended for use in VHF pre-amplifiers where linear, low-noise amplification is required. Its extremely low feedback capacitance permits high stable gain without the use of neutralization.

The 3N205 is intended for use as a VHF mixer and is well suited for TV tuners. Its use as a mixer minimizes cross-modulation distortion and provides low-noise operation.

The 3N206 is designed for application in tuned high-frequency amplifiers such as TV IF strips. Its extremely low feedback capacitance permits high stage gain and stability without the necessity for neutralization.

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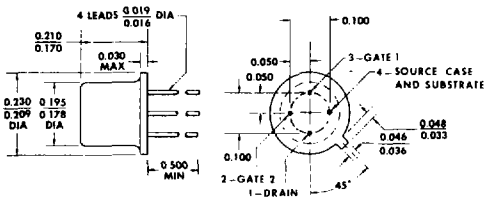
*mechanical data

THE SUBSTRATE AND SOURCE ARE IN ELECTRICAL CONTACT WITH THE CASE



ALL DIMENSIONS ARE IN INCHES UNLESS OTHERWISE SPECIFIED

ALL JEDEC TO-72 DIMENSIONS AND NOTES ARE APPLICABLE

*absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

Drain–Gate-One Voltage	30 V
Drain–Gate-Two Voltage	30 V
Drain-Source Voltage	25 V
Forward Gate-One-Terminal Current (See Note 1)	10 mA
Forward Gate-Two-Terminal Current (See Note 1)	10 mA
Reverse Gate-One-Terminal Current	−10 mA
Reverse Gate-Two-Terminal Current	−10 mA
Continuous Drain Current	50 mA
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 2)	360 mW
Continuous Device Dissipation at (or below) 25°C Case Temperature (See Note 3)	1.2 W
Storage Temperature Range	−65°C to 200°C
Lead Temperature 1/16 Inch from Case for 10 Seconds	300°C

NOTES: 1. Forward gate-terminal current is the current into a gate terminal with a forward gate-source voltage applied. This voltage is of such polarity that an increase in its magnitude causes the channel resistance to decrease.
2. Derate linearly to 175°C free-air temperature at the rate of 2.4 mW/°C.
3. Derate linearly to 175°C case temperature at the rate of 8 mW/°C.

*JEDEC registered data. This data sheet contains all applicable registered data in effect at the time of publication.

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*electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	MAX	UNIT
$V_{(BR)DS}$	Drain-Source Breakdown Voltage	I_D = 10 μA,	$V_{G1S} = V_{G2S}$ = −5 V		25		V
$V_{(BR)G1SSF}$	Gate-One–Source Forward Breakdown Voltage	I_{G1} = 10 mA,	$V_{G2S} = V_{DS}$ = 0,	See Note 4	6	30	V
$V_{(BR)G1SSR}$	Gate-One–Source Reverse Breakdown Voltage	I_{G1} = −10 mA,	$V_{G2S} = V_{DS}$ = 0,	See Note 4	−6	−30	V
$V_{(BR)G2SSF}$	Gate-Two–Source Forward Breakdown Voltage	I_{G2} = 10 mA,	$V_{G1S} = V_{DS}$ = 0,	See Note 4	6	30	V
$V_{(BR)G2SSR}$	Gate-Two–Source Reverse Breakdown Voltage	I_{G2} = −10 mA,	$V_{G1S} = V_{DS}$ = 0,	See Note 4	−6	−30	V
I_{G1SSF}	Gate-One-Terminal Forward Current	V_{G1S} = 5 V,	$V_{G2S} = V_{DS}$ = 0			10	nA
I_{G1SSR}	Gate-One-Terminal Reverse Current	V_{G1S} = −5 V,	$V_{G2S} = V_{DS}$ = 0			−10	nA
		V_{G1S} = −5 V,	$V_{G2S} = V_{DS}$ = 0,	T_A = 150°C		−10	μA
I_{G2SSF}	Gate-Two-Terminal Forward Current	V_{G2S} = 5 V,	$V_{G1S} = V_{DS}$ = 0			10	nA
I_{G2SSR}	Gate-Two-Terminal Reverse Current	V_{G2S} = −5 V,	$V_{G1S} = V_{DS}$ = 0			−10	nA
		V_{G2S} = −5 V,	$V_{G1S} = V_{DS}$ = 0,	T_A = 150 C		−10	μA
I_{DS}	Zero-Gate-One-Voltage Drain Current	V_{DS} = 15 V, V_{G2S} = 4 V,	V_{G1S} = 0, See Note 5	3N204 3N205	6	30	mA
				3N206	3	15	
$V_{G1S(off)}$	Gate-One–Source Cutoff Voltage	V_{DS} = 15 V,	V_{G2S} = 4 V,	I_D = 20 μA	−0.5	−4	V
$V_{G2S(off)}$	Gate-Two–Source Cutoff Voltage	V_{DS} = 15 V,	V_{G1S} = 0,	I_D = 20 μA	−0.2	−4	V
$\|y_{fs}\|$	Small-Signal Common-Source Forward Transfer Admittance	V_{DS} = 15 V, V_{G2S} = 4 V, See Note 6	V_{G1S} = 0, f = 1 kHz,	3N204 3N205	10	22	mmho
				3N206	7	17	
C_{rss}	Common-Source Short-Circuit Reverse Transfer Capacitance	V_{DS} = 15 V, f = 1 MHz	V_{G2S} = 4 V,	I_D = 10 mA,	0.005	0.03	pF

NOTES: 4. All gate breakdown voltages are measured while the device is conducting rated gate current. This ensures that the gate-voltage-limiting network is functioning properly.

5. This parameter must be measured using pulse techniques. t_w = 300 μs, duty cycle ≤ 2%.

6. This parameter must be measured with bias voltages applied for less than 5 seconds to avoid overheating.

*3N204 operating characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS		3N204 MIN	3N204 TYP	3N204 MAX	UNIT
F	Common-Source Spot Noise Figure	V_{DD} = 18 V, f = 200 MHz,	V_{GG} = 7 V, See Figure 1			3.5	dB
G_{ps}	Small-Signal Common-Source Insertion Power Gain			20		28	dB
B	Bandwidth			7		12	MHz
$V_{GG(GC)}$	Gain-Control Gate-Supply Voltage	V_{DD} = 18 V, f = 200 MHz,	ΔG_{ps} = −30 dB†, See Figure 1	0		−2	V
F	Common-Source Spot Noise Figure	V_{DS} = 15 V, I_D = 10 mA, See Figures 2 and 4	V_{G2S} = 4 V, f = 450 MHz,			5	dB
G_{ps}	Small-Signal Common-Source Insertion Power Gain			14			dB
F	Common-Source Spot Noise Figure	V_{DS} = 15 V, I_D = 10 mA, See Figures 3 and 5	V_{G2S} ≈ 4 V, f = 900 MHz,		7		dB
G_{ps}	Small-Signal Common-Source Insertion Power Gain				12		dB

†ΔG_{ps} is defined as the change in G_{ps} from the value at V_{GG} = 7 volts.

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*3N205 operating characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS	3N205 MIN	3N205 MAX	UNIT
$G_{ps(conv)}$	Small-Signal Conversion Power Gain	V_{DD} = 18 V, f_{LO} = 245 MHz‡,	17	28	dB
B	Bandwidth	f_{RF} = 200 MHz, See Figure 6	4	7	MHz

‡Amplitude at input from local oscillator is 3 volts rms.

*3N206 operating characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS	3N206 MIN	3N206 MAX	UNIT
F	Common-Source Spot Noise Figure	V_{DD} = 24 V, V_{GG} = 6 V, f = 45 MHz, See Figure 7		4	dB
G_{ps}	Small-Signal Common-Source Insertion Power Gain		25	35	dB
B	Bandwidth		3	6	MHz
$V_{GG(GC)}$	Gain-Control Gate-Supply Voltage	V_{DD} = 24 V, ΔG_{ps} = −30 dB§, f = 45 MHz, See Figure 7		+0.6 −1.6	V

§G_{ps} is defined as the change in G_{ps} from the value at V_{GG} = 6 volts.

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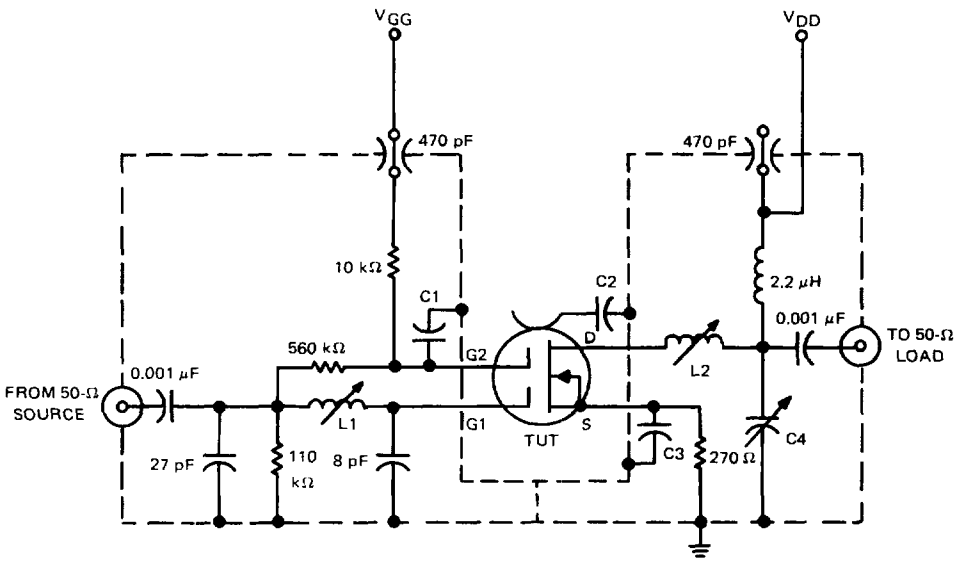
PARAMETER MEASUREMENT INFORMATION



CIRCUIT COMPONENT INFORMATION

C1, C2, & C3: Leadless disc ceramic, 0.001 μF
C4: ARCO 462, 5-80 pF, or equivalent
L1: 3T #18, 3/16-inch-dia aluminum slug
L2: 9T #20, 3/16-inch-dia aluminum slug

FIGURE 1—200-MHz POWER GAIN, GAIN CONTROL VOLTAGE, AND NOISE FIGURE TEST CIRCUIT FOR 3N204*

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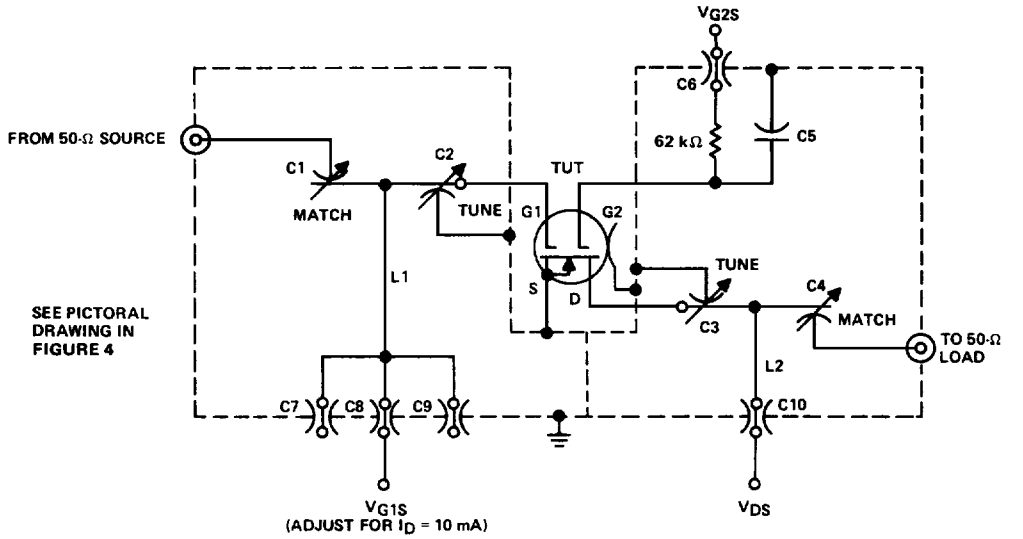
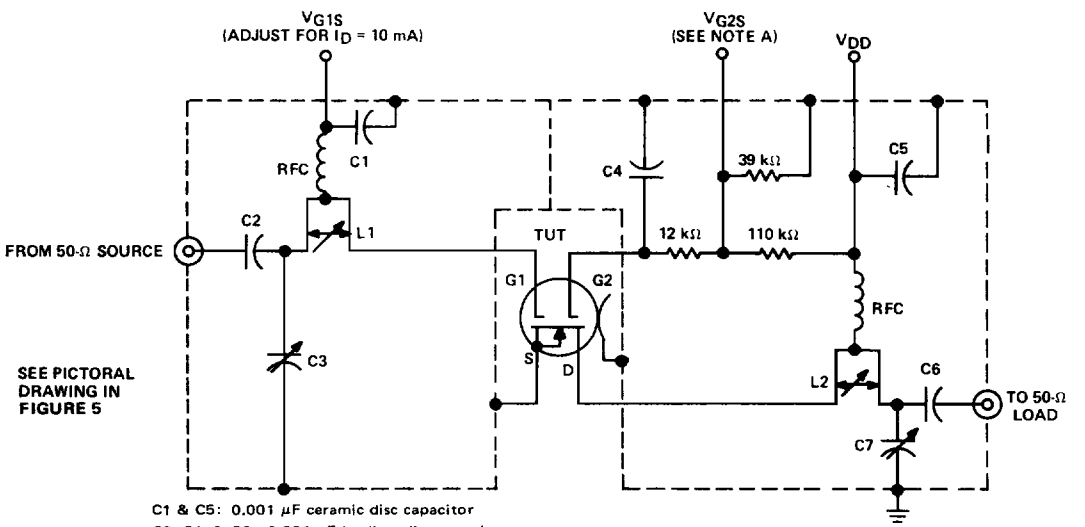
PARAMETER MEASUREMENT INFORMATION



CIRCUIT COMPONENT INFORMATION

C1 thru C4: See Figure 30, Note D
C5: 0.001 μF leadless disc capacitor
C6 thru C10: Allen-Bradley F5AU 0.001 μF feed-through capacitors
L1 & L2: See Figure 30

FIGURE 2–450-MHz POWER GAIN AND NOISE TEST CIRCUIT FOR 3N204*



C1 & C5: 0.001 μF ceramic disc capacitor
C2, C4, & C6: 0.001 μF leadless disc capacitor
C3 & C7: Johanson 3901, 1-15 pF, or equivalent
L1 & L2 are 1/4 inch slotted cyclinders, 3/16 inch inside diameter, with a shorting ring adjusted by a nylon screw. Minimum slot lengths are 3/4 inch for L1 and 1 inch for L2.
RFC: 10T #30, 3/16 inch dia, 5/16 inch in length

NOTE A: This terminal is provided for gain control, if desired. If not used for this purpose, it should be left open.

*JEDEC registered data

FIGURE 3–900-MHz POWER GAIN AND NOISE TEST CIRCUIT FOR 3N204

NOTES:
A. All dimensions are in inches.
B. The removable top of test fixture is not shown.
C. For clarity, the 62 kΩ resistor, the source and gate-2 socket pins, and insulating stand-off terminals (ISOT) soldered into the fold of L1 and L2 respectively for mechanical support, are not shown in view A.
D. C1 and C2 (C3 and C4) consist of shim brass and the "C" portion of L1 (L2) separated by air and the mylar tape covering the "C" portion of L1 (L2).

NOTE:
E. The four views surrounding the center view are as they would appear before the metal is bent up to form the sides.

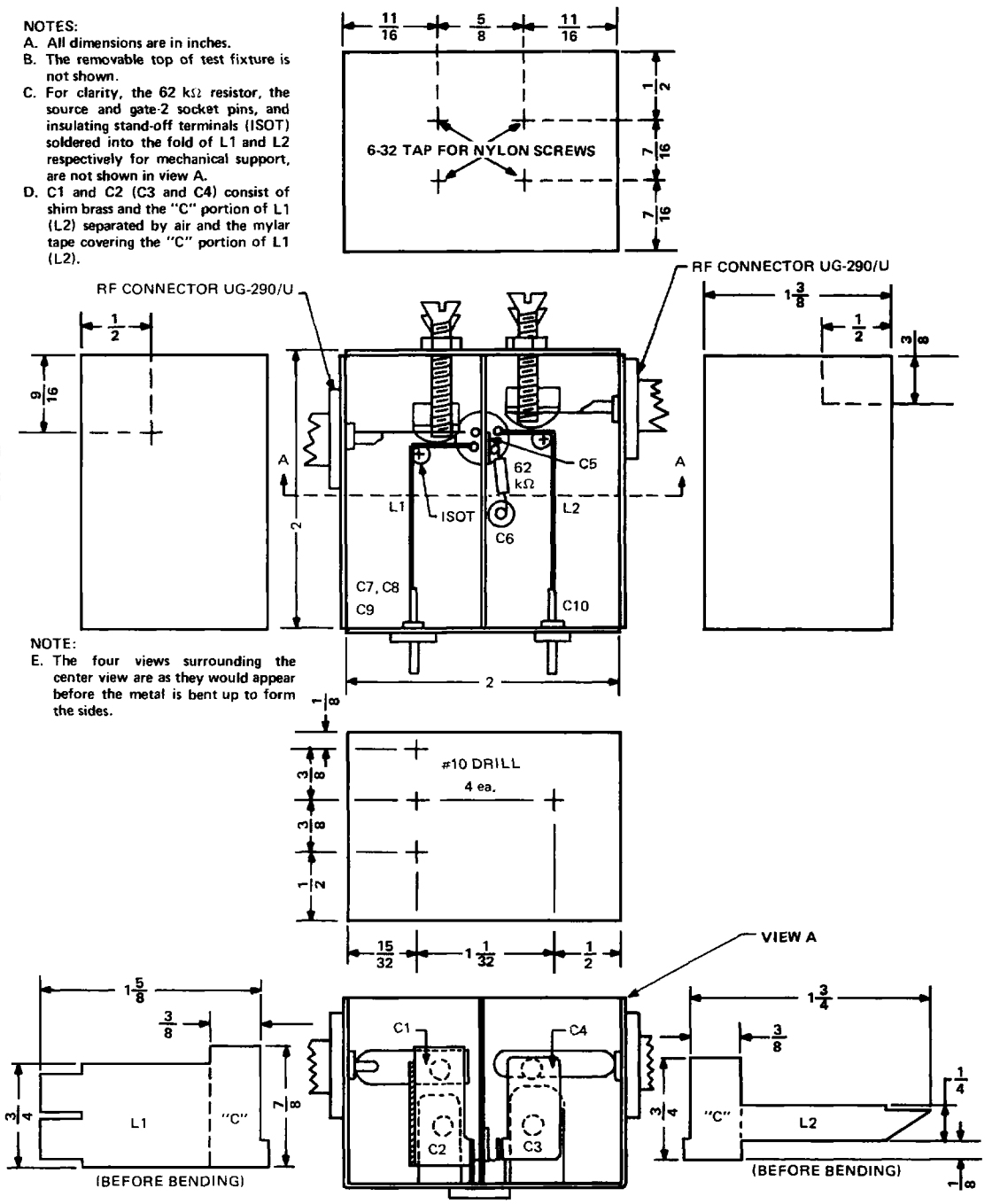


FIGURE 4–450-MHz POWER GAIN AND NOISE TEST FIXTURE*

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NOTES:
A. All dimensions are in inches.
B. The removable top of test fixture is not shown.
C. L1 and L2 are attached to the back of the test fixture by insulating stand-off terminals (ISOT) located as shown.
D. The four views surrounding the center view are as they would appear *before the metal is bent up to form the sides.*

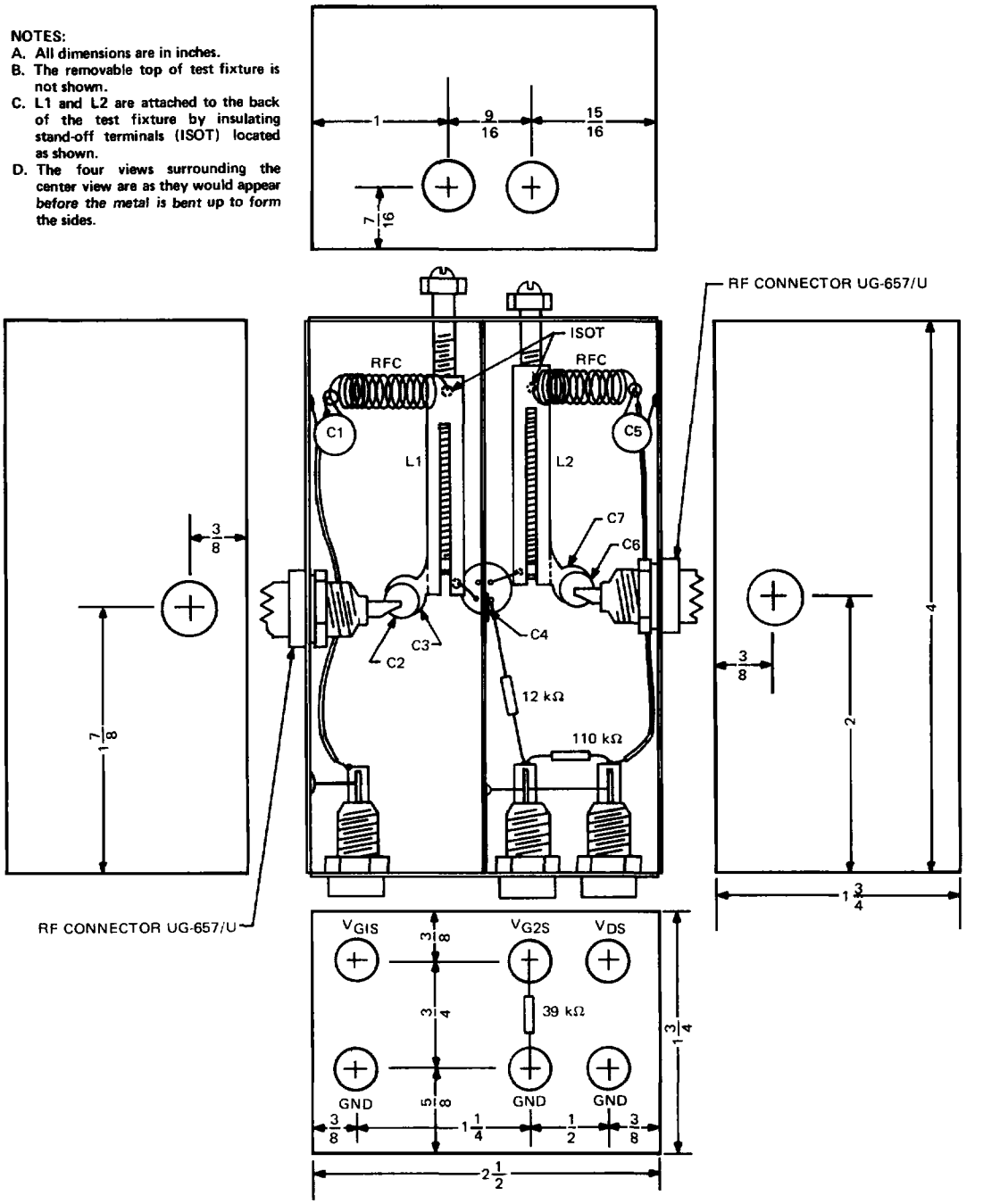
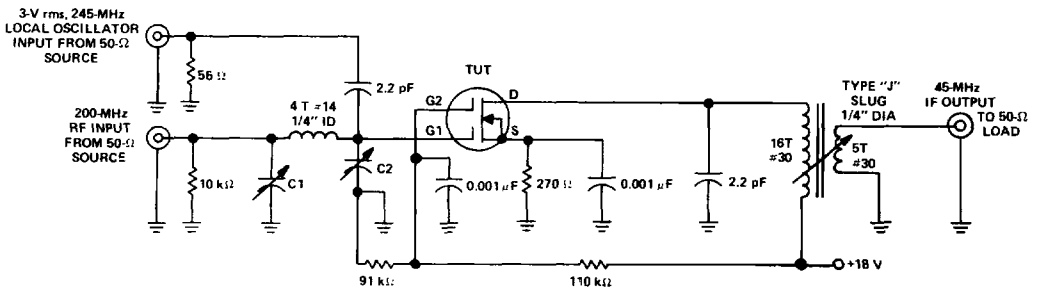


FIGURE 5–900-MHz POWER GAIN AND NOISE TEST FIXTURE

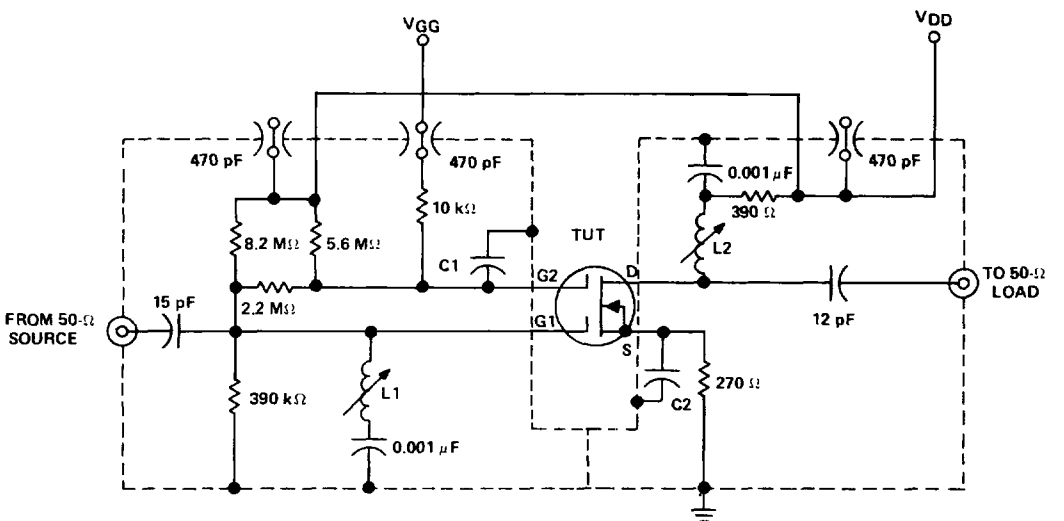
PARAMETER MEASUREMENT INFORMATION



CIRCUIT COMPONENT INFORMATION

C1: Arco 404 (or equivalent), 8 to 60 pF
C2: Arco 400 (or equivalent), 0.9 to 7 pF

FIGURE 6—200-MHz-to-45-MHz CIRCUIT FOR CONVERSION POWER GAIN FOR 3N205*



CIRCUIT COMPONENT INFORMATION

C1: Leadless disc ceramic, 0.001 μF
C2: Leadless disc ceramic, 0.01 μF
L1: 8T # 28, 5/32 inch-dia form, type "J" slug
L2: 9T # 28, 5/32-inch-dia form, type "J" slug

FIGURE 7—45-MHz POWER GAIN AND NOISE FIGURE TEST CIRCUIT FOR 3N206*

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TYPICAL CHARACTERISTICS AT T_A = 25°C

3N204
RELATIVE SMALL-SIGNAL POWER GAIN vs GAIN-CONTROL GATE-SUPPLY VOLTAGE

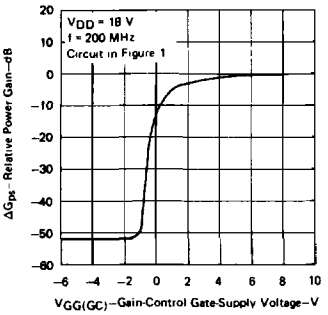

FIGURE 8

3N204
SMALL-SIGNAL COMMON-SOURCE INSERTION POWER GAIN vs DRAIN CURRENT

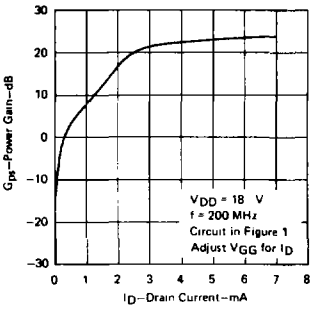

FIGURE 9

3N204
COMMON-SOURCE SPOT NOISE FIGURE vs GAIN-CONTROL GATE-SUPPLY VOLTAGE

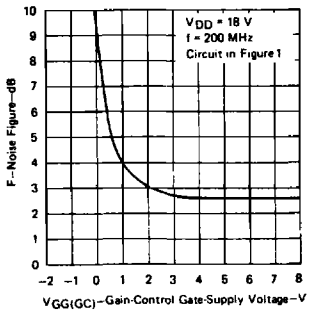

FIGURE 10

3N204
OPTIMUM SPOT NOISE FIGURE vs FREQUENCY

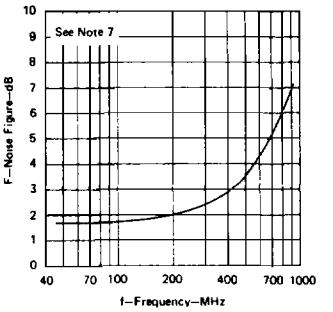

FIGURE 11

3N205
SMALL-SIGNAL CONVERSION POWER GAIN vs *INPUT FROM LOCAL OSCILLATOR*

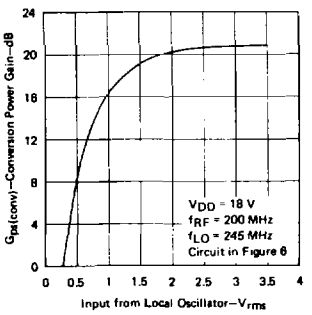

FIGURE 12

3N206
SMALL-SIGNAL COMMON-SOURCE INSERTION POWER GAIN vs *GAIN-CONTROL GATE-SUPPLY VOLTAGE*

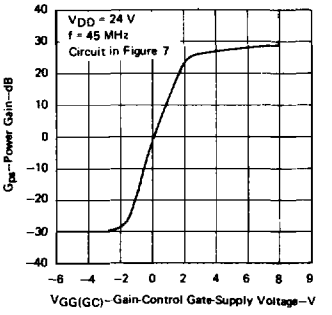

FIGURE 13

NOTE 7: Test conditions at 45 MHz, 200 MHz, 450 MHz, and 900 MHz are the conditions given in the tables of operating characteristics for 3N204 and 3N206.

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