

J175 / J176 / MMBFJ175 / MMBFJ176 / MMBFJ177 P-Channel Switch

Description

This device is designed for low-level analog switching sample-and-hold circuits and chopper-stabilized amplifiers. Sourced from process 88.

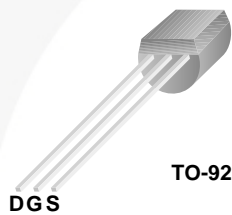


Figure 1. J175 / J176 Device Package

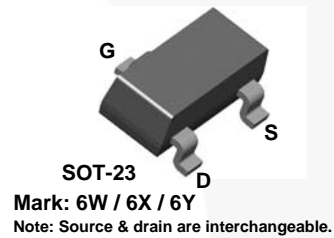


Figure 2. MMBFJ175 / 176 / 177 Device Package

Ordering Information

| Part Number | Marking | Package | Packing Method |
|-------------|---------|-----------|----------------|
| J175_D26Z | J175 | TO-92 3L | Tape and Reel |
| J176_D74Z | J176 | TO-92 3L | Ammo |
| MMBFJ175 | 6W | SOT-23 3L | Tape and Reel |
| MMBFJ176 | 6X | SOT-23 3L | Tape and Reel |
| MMBFJ177 | 6Y | SOT-23 3L | Tape and Reel |

Absolute Maximum Ratings^{(1),(2)}

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Values are at $T_A = 25^\circ\text{C}$ unless otherwise noted.

| Symbol | Parameter | Value | Unit |
|----------------|--|--------------|------------------|
| V_{DG} | Drain-Gate Voltage | -30 | V |
| V_{GS} | Gate-Source Voltage | 30 | V |
| I_{GF} | Forward Gate Current | 50 | mA |
| T_J, T_{STG} | Operating and Storage Junction Temperature Range | -55 to + 150 | $^\circ\text{C}$ |

Notes:

1. These ratings are based on a maximum junction temperature of 150°C .
2. These are steady-state limits. Fairchild Semiconductor should be consulted on applications involving pulsed or low-duty cycle operations.

Thermal Characteristics⁽³⁾

Values are at $T_A = 25^\circ\text{C}$ unless otherwise noted.

| Symbol | Parameter | Max. | | Unit |
|-----------------|---|-------------|--------------------------------------|---------------------------|
| | | J175 / J176 | MMBFJ175 / MMBFJ176 / MMBFJ177 | |
| P_D | Total Device Dissipation | 350 | 225 | mW |
| | Derate Above 25°C | 2.8 | 1.8 | mW/ $^\circ\text{C}$ |
| $R_{\theta JC}$ | Thermal Resistance, Junction to Case | 125 | | $^\circ\text{C}/\text{W}$ |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient | 357 | 556 | $^\circ\text{C}/\text{W}$ |

Note:

3. PCB size: FR-4 76 x 114 x 1.57 mm³ (3.0 inch x 4.5 inch x 0.062 inch) with minimum land pattern size.

Electrical Characteristics

Values are at $T_A = 25^\circ\text{C}$ unless otherwise noted.

| Symbol | Parameter | Conditions | Min. | Max. | Unit | |
|----------------------------|--|--|--------------------|------|-------|----------|
| Off Characteristics | | | | | | |
| $V_{(BR)GSS}$ | Gate-Source Breakdown Voltage | $I_G = 1.0 \mu\text{A}, V_{DS} = 0$ | 30 | | V | |
| I_{GSS} | Gate Reverse Current | $V_{GS} = 20 \text{ V}, V_{DS} = 0$ | | 1.0 | nA | |
| $V_{GS(off)}$ | Gate-Source Cut-Off Voltage | $V_{DS} = -15 \text{ V}, I_D = -10 \text{ nA}$ | J175 / MMBFJ175 | 3.0 | 6.0 | V |
| | | | J176 / MMBFJ176 | 1.0 | 4.0 | |
| | | | MMBFJ177 | 0.8 | 2.5 | |
| On Characteristics | | | | | | |
| I_{DSS} | Zero-Gate Voltage Drain Current ⁽⁴⁾ | $V_{DS} = -15 \text{ V}, I_{GS} = 0$ | J175 / MMBFJ175 | -7.0 | -60.0 | mA |
| | | | J176 / MMBFJ176 | -2.0 | -25.0 | |
| | | | MMBFJ177 | -1.5 | -20.0 | |
| $r_{DS(on)}$ | Drain-Source On Resistance | $V_{DS} \leq 0.1 \text{ V}, V_{GS} = 0$ | J175 / MMBFJ175 | | 125 | Ω |
| | | | J176 / MMBFJ176 | | 250 | |
| | | | MMBFJ177 | | 300 | |

Note:

4. Pulse test: pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2.0\%$.

Typical Performance Characteristics

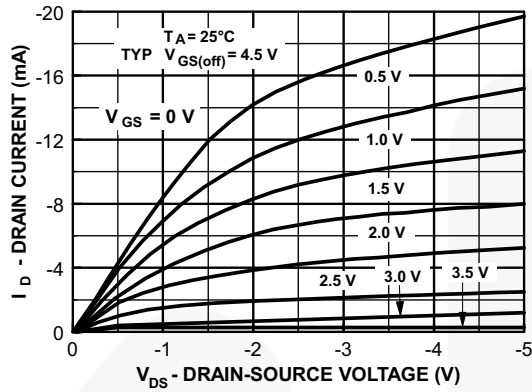


Figure 3. Common Drain-Source

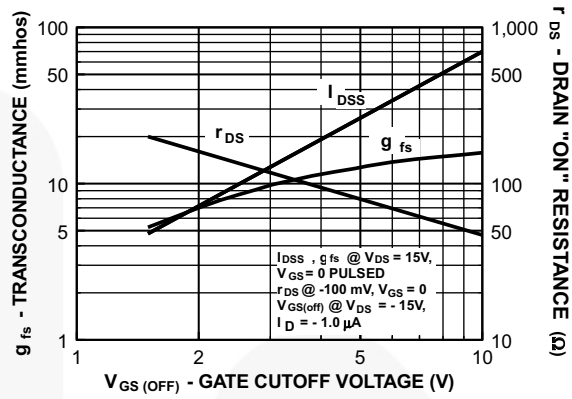


Figure 4. Parameter Interactions

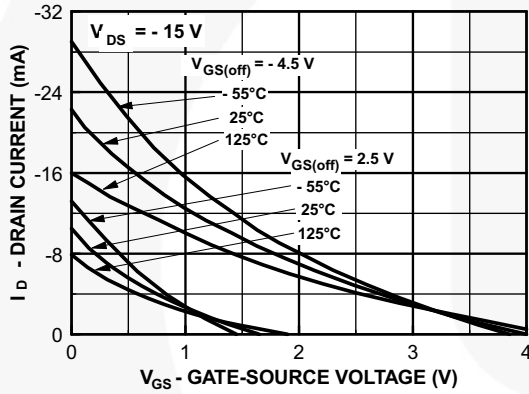


Figure 5. Transfer Characteristics

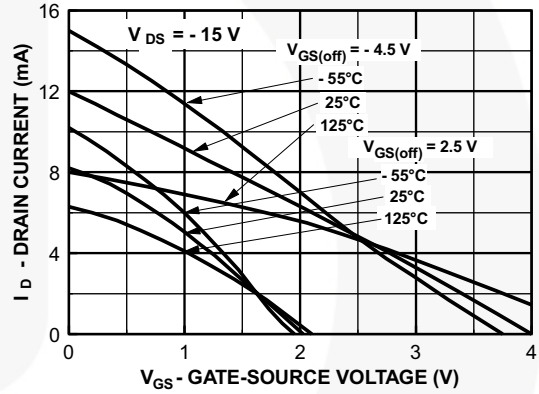


Figure 6. Transfer Characteristics

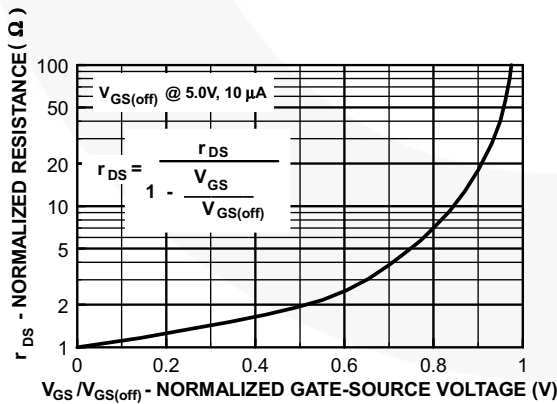


Figure 7. Normalized Drain Resistance vs. Bias Voltage

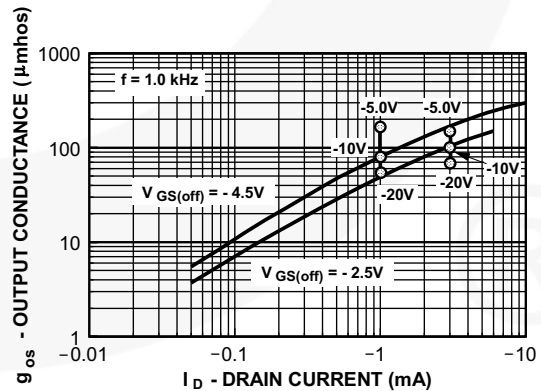


Figure 8. Output Conductance vs. Drain Current

Typical Performance Characteristics (Continued)

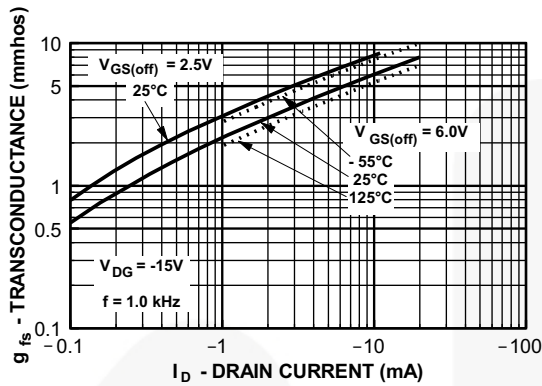


Figure 9. Transconductance vs. Drain Current

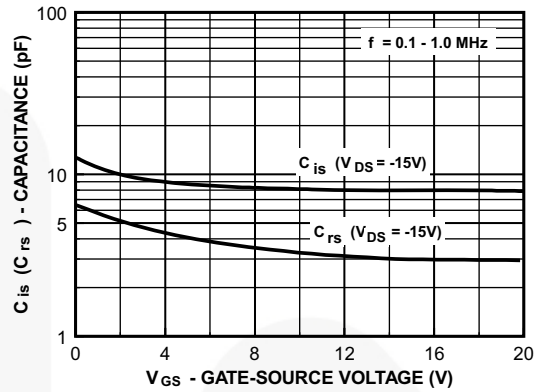


Figure 10. Capacitance vs. Voltage

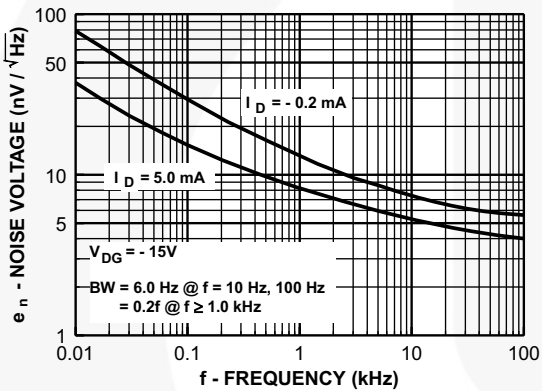


Figure 11. Noise Voltage vs. Frequency

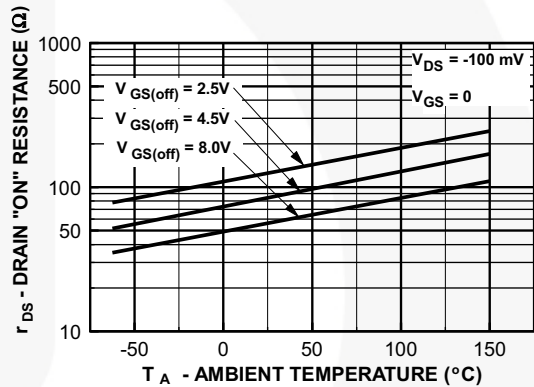


Figure 12. Channel Resistance vs. Temperature

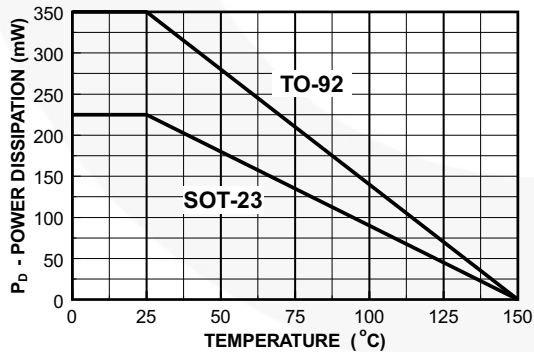
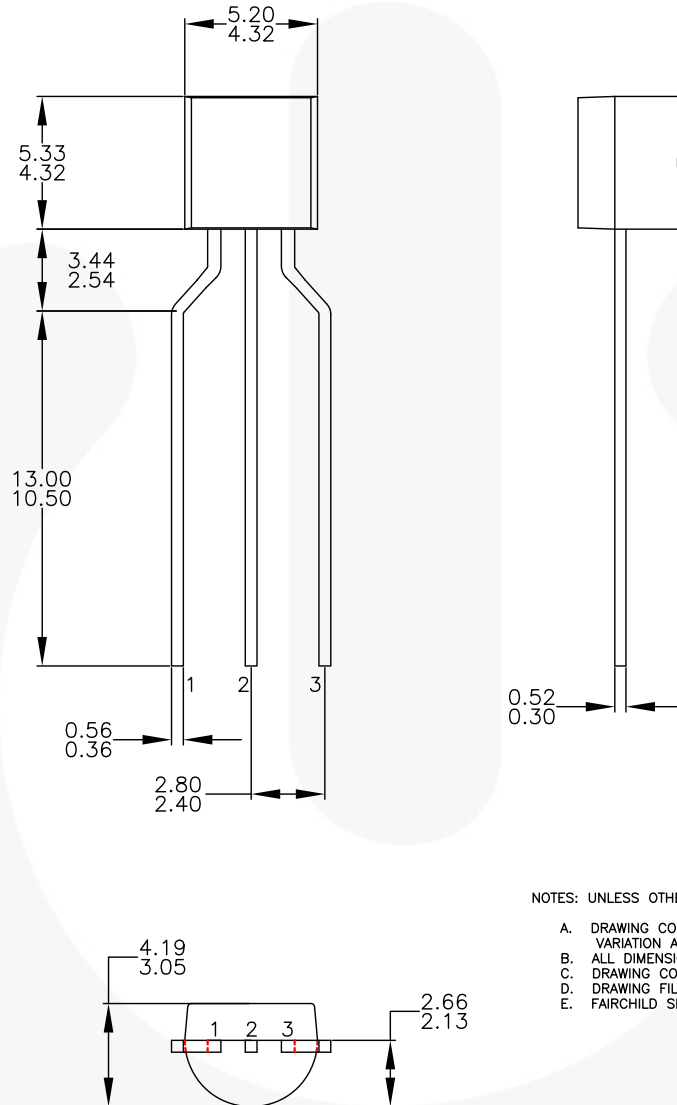


Figure 13. Power Dissipation vs. Ambient Temperature

Physical Dimensions

TO-92



NOTES: UNLESS OTHERWISE SPECIFIED

- A. DRAWING CONFORMS TO JEDEC MS-013, VARIATION AC.
- B. ALL DIMENSIONS ARE IN MILLIMETERS.
- C. DRAWING CONFORMS TO ASME Y14.5M-2009.
- D. DRAWING FILENAME: MKT-ZA03FREV3.
- E. FAIRCHILD SEMICONDUCTOR.

Figure 14. 3-LEAD, TO92, MOLDED, 0.200 IN LINE SPACING LEAD FORM (J61Z OPTION) (ACTIVE)

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Physical Dimensions (Continued)

SOT-23

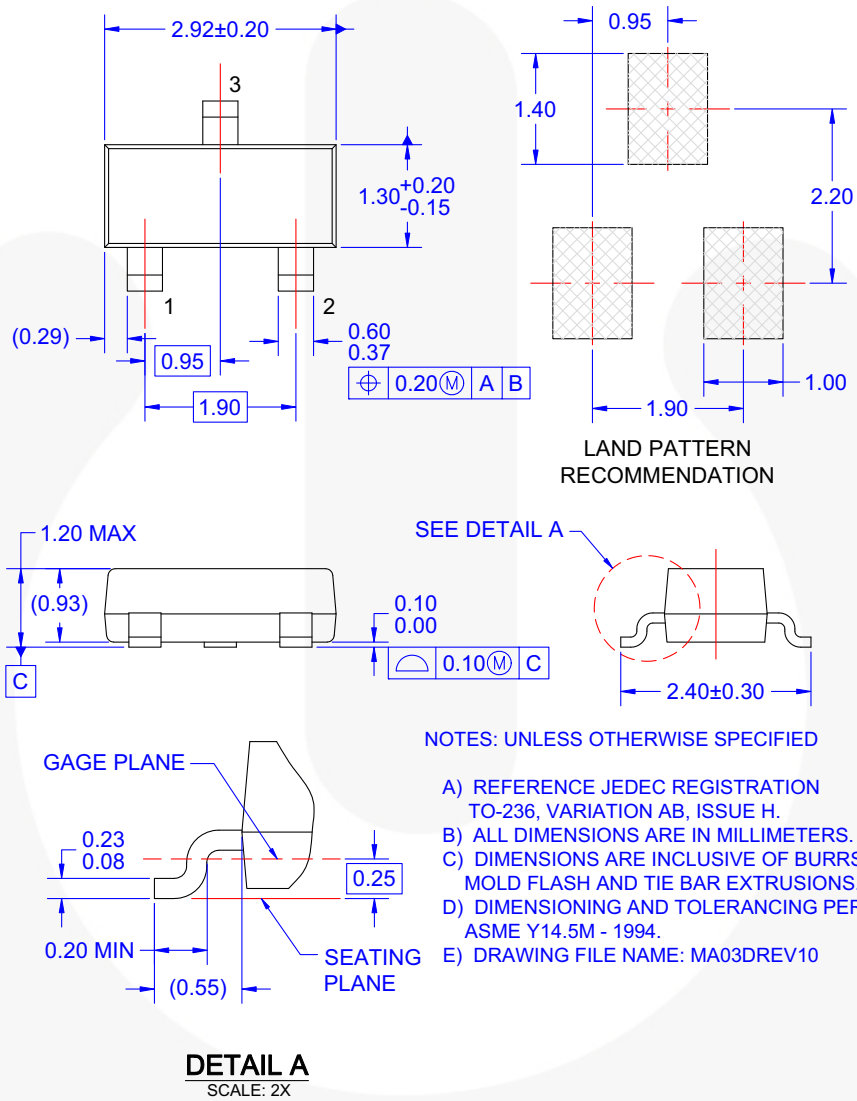


Figure 15. 3-LEAD, SOT23, JEDEC TO-236, LOW PROFILE (ACTIVE)

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