CA3179

T-45-19-13

1.25 GHz Prescaler

For Industrial Applications

FEATURES:
- *Broadband operation - DC to 1.25 GHz*
- *High sensitivity*
- *Standard T^2L or ECL power supply*
- *Dual mode operation - VHF/UHF (÷ 64/ ÷ 256)*
- *Complementary ECL outputs*
- *Independent VHF and UHF input terminals*

The RCA-CA3179E is an integrated-circuit prescaler intended for use in communications and instrumentation systems. It performs division by 256 in the uhf mode and division by 64 in the vhf mode.

The mode of operation is selected by means of the bandswitch and the separate uhf and vhf input terminals provided. Either single- or double-ended inputs can be applied. These inputs are normally ac coupled, but dc coupling can be used if the specified bias levels are maintained. The output is a complementary emitter-coupled stage capable of driving a 33-pF or equivalent load. The harmonic output is reduced above 40 MHz by limiting output-signal rise and fall times and by maintaining a balanced load.

In the uhf mode, which is activated by applying a high level (logical 1) to the bandswitch input terminal, all eight divider stages are operative, resulting in division by 256. In the vhf mode, activated by a low level (logical 0) at the vhf input terminal, two divider stages are bypassed, resulting in division by 64. An internal amplifier/multiplexer provides this control while isolating both inputs, amplifying the input signal, and improving sensitivity.

The CA3179E is supplied in the 14-lead dual-in-line plastic package.

Applications:
- *Digital frequency synthesizers for:*
  - *VHF/UHF receivers*
  - *Satellite communications*
  - *Instrumentation*
- *High-frequency divider for:*
  - *UHF frequency counters*
  - *UHF timers*
  - *High-speed computers*
  - *Frequency standards*
  - *SHF second IF local-oscillator injection*
  - *PCM communications*
  - *Satellite communications*
  - *Radar ranging systems*
- *High-frequency up-converters*

Table of Absolute-Maximum Ratings

Term. No.	Min. Volts	Max. Volts	Max. I_{IN} (mA)	Max. I_{OUT} (mA)
1 & 2*	0	5.5	110	0
3	−0.3	20	1	1
4 & 5	—	—	0.1	10
9, 10, 13, 14▲	—	4	0.1	1

*Terms. 1 & 2 tied together.
▲Maximum rf drive = 500 mVRMS.
Terms. 7 & 8 are system ground and tied together.
Terms. 6, 11, 12 = no connection.

File Number **1176**

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MAXIMUM RATINGS, ***Absolute-Maximum Values:***

DC SUPPLY VOLTAGE ..... 5.5 V
DC BANDSWITCH VOLTAGE ..... 20 V
RMS INPUT VOLTAGE ..... 0.5 V
DEVICE DISSIPATION:
  UP TO T_A = 70°C ..... 700 mW
  ABOVE T_A = 70°C ..... derate linearly at 11.1 mW/°C
AMBIENT TEMPERATURE RANGE:
  OPERATING ..... 0 to 85°C
  STORAGE ..... −55 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
  AT DISTANCE 1/16 ± 1/32 INCH (1.59 ± 0.79 MM)
  FROM CASE FOR 10 SECONDS MAX. ..... +265°C

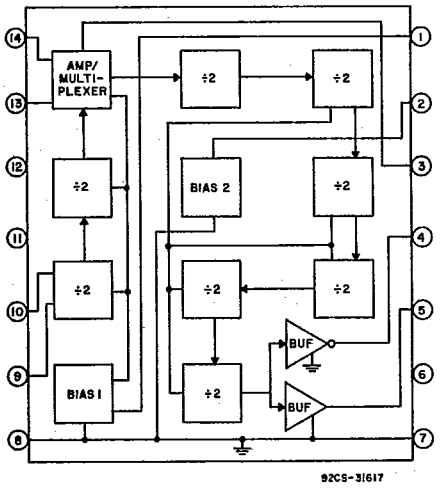


Fig. 1 - CA3179 block diagram.

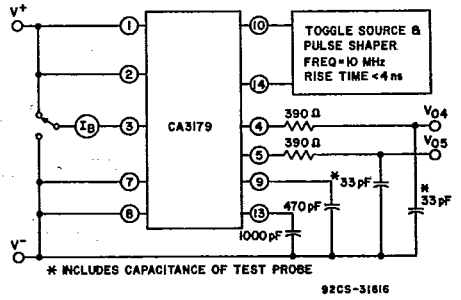


Fig. 2 - DC characteristics test circuit.

ELECTRICAL CHARACTERISTICS at T_A = 25°C, V+ = 5 V, V− = 0 V

CHARACTERISTIC	TEST CONDITIONS	LIMITS Min.	Typ.	Max.	UNITS
Static (See Fig. 2)					
Supply Current, I+	Terms. 1 & 2	30	65	100	mA
Bandswitch Voltage: Low, V_{BL}	Term. 3	2.4	—	—	V
Bandswitch Voltage: High, V_{BH}	Term. 3	—	—	0.8	V
Bandswitch Current: Low, I_{BL}	V3 = 0 V	−1	—	—	mA
Bandswitch Current: High, I_{BH}	V3 = 20 V	—	—	0.5	mA
Dynamic (See Fig. 3)					
Sine Wave Sensitivity (Single-ended)	f_{IN} = 450 to 950 MHz, V3 = 5 V	0	30	80	mVRMS
Sine Wave Sensitivity (Single-ended)	f_{IN} = 80 to 450 MHz, V3 = 5 V	—	50	160	mVRMS
Sine Wave Sensitivity (Single-ended)	f_{IN} = 90 to 275 MHz, V3 = 0 V	—	5	40	mVRMS
Output Voltage: High, V_{OH}	Term. 4 or 5	—	4.2	—	V
Output Voltage: Low, V_{OL}	Term. 4 or 5	—	3	—	V
Output Voltage: Peak-to-Peak, V_{OP-P}	Term. 4 or 5	0.65	1.1	1.6	V
Output Rise or Fall Time, t_r,t_f		40	70	110	ns
Internal Bias	Term. 13 or 14	$(V_{DD} - 1)$			V
Internal Bias	Term. 9 or 10	$(V_{DD} - 2.7)$			V
DC Input Resistance, R_I	Term. 13 to 14	2000			Ω
DC Input Resistance, R_I	Term. 9 to 10	1000			Ω
Complex Input Impedance	Term.9 to 10, V_{IN} = 100 mV, f_{IN} = 950 MHz	20			Ω
Complex Input Impedance	Term.9 to 10, V_{IN} = 100 mV, f_{IN} = 450 MHz	30 - j80			Ω
Complex Input Impedance	Term.13 to 14, V_{IN} = 100mV, f_{IN} = 275 MHz	35 - j100			Ω

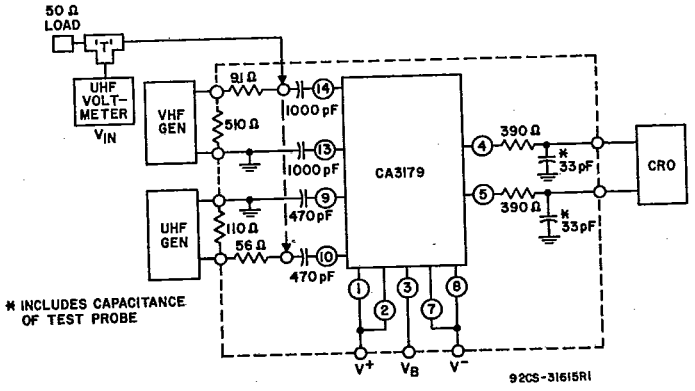


Fig. 3 - AC characteristics test circuit.

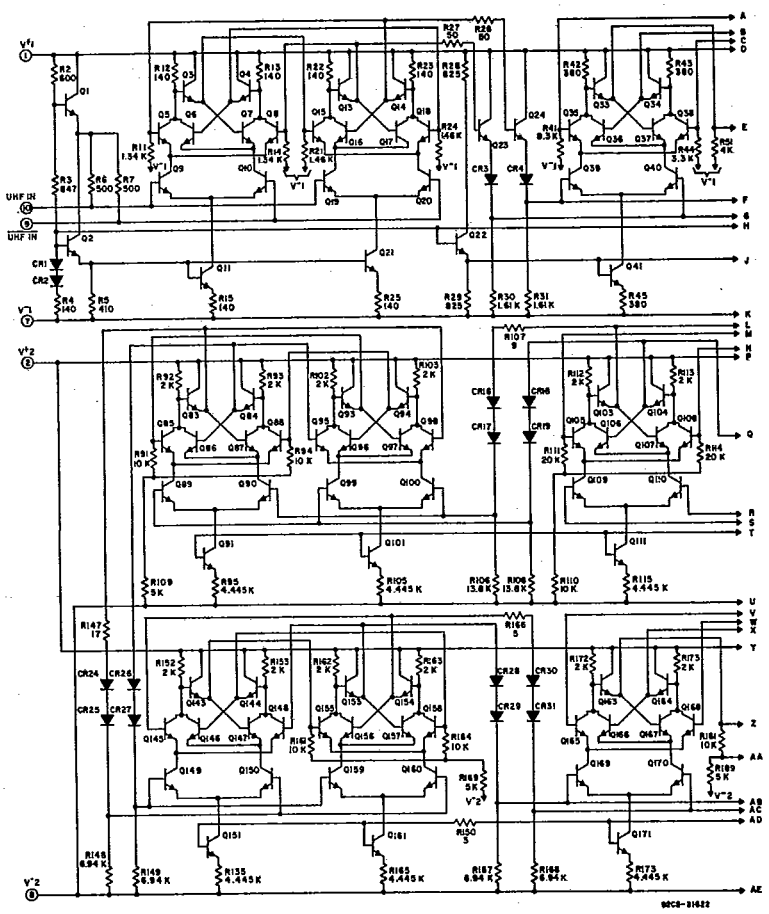


Fig. 4 - Schematic diagram (cont'd on next page).

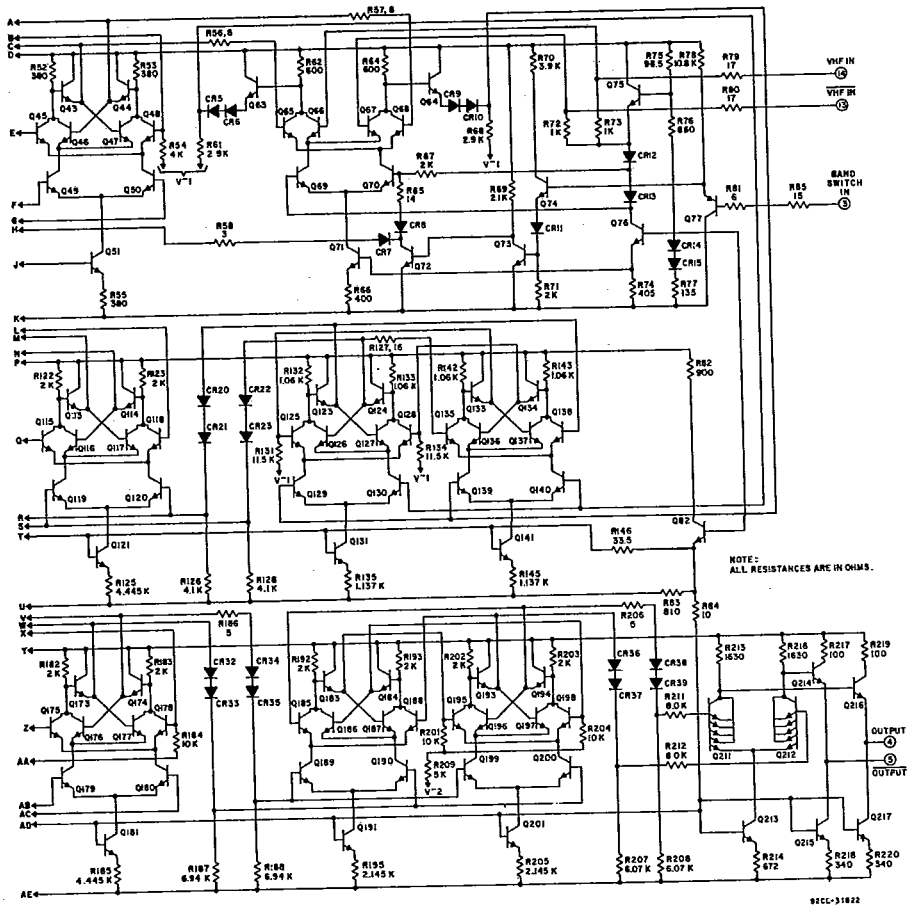


Fig. 4 – Schematic diagram (cont'd from previous page).

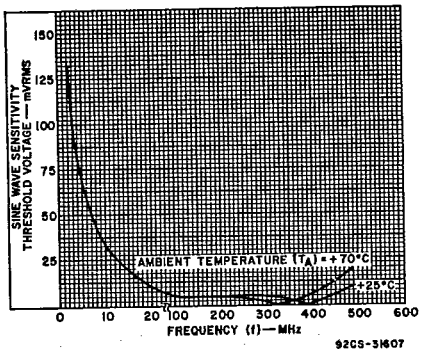


Fig. 5 - Typical threshold sensitivity in the +64 VHF mode.

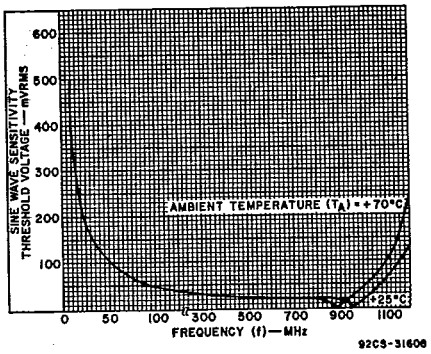


Fig. 6 - Typical threshold sensitivity in the +256 UHF mode.

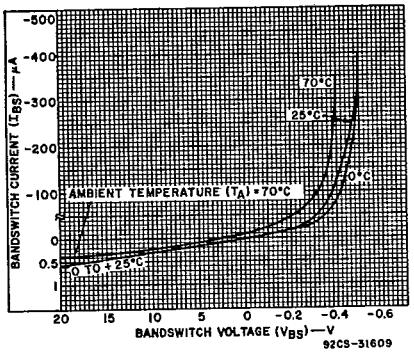


Fig. 7 - Typical bandswitch current as a function of bandswitch voltage and ambient temperature.

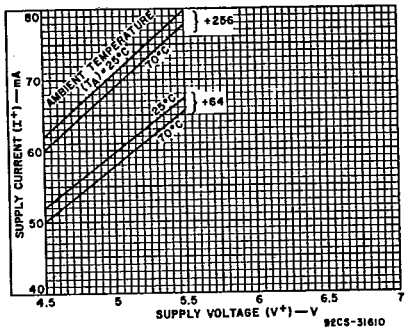


Fig. 8 - Supply current as a function of supply voltage and ambient temperature.

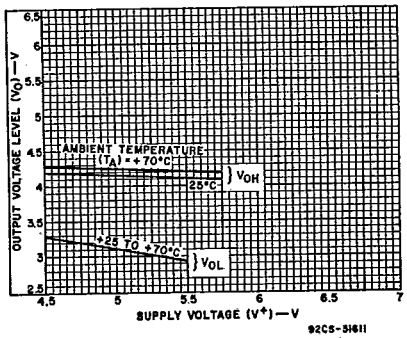


Fig. 9 - Typical output voltage level as a function of supply voltage and ambient temperature.

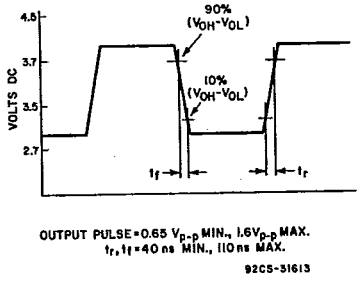


Fig. 10 - Output pulse characteristics.

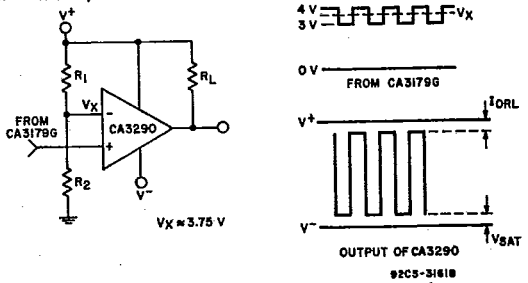


Fig. 11 - Typical bipolar interface circuit.

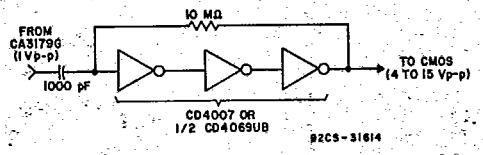
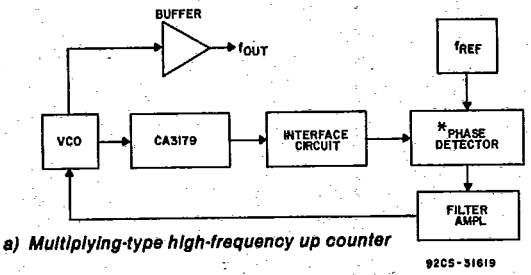
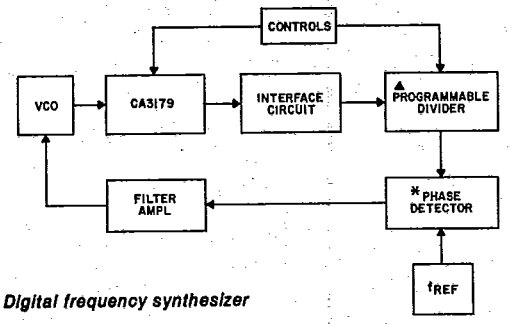


Fig. 12 - Typical CMOS interface circuit.



a) Multiplying-type high-frequency up counter



b) Digital frequency synthesizer

* CD4046A/B, CD4030A/B, CD4070A/B OR EQUIVALENT
▲ CD4018B, CD4029B, CD4059A, CD40102B, CD40103B OR EQUIVALENT
92CS-31620

Fig. 13 - Typical system configuration.

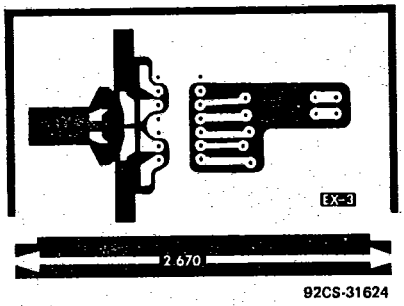


Fig. 14 - Printed-circuit board for the dynamic test circuit.

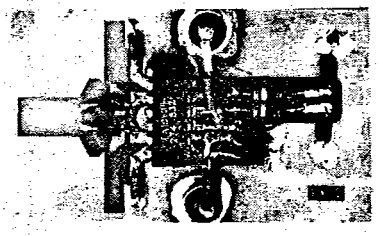
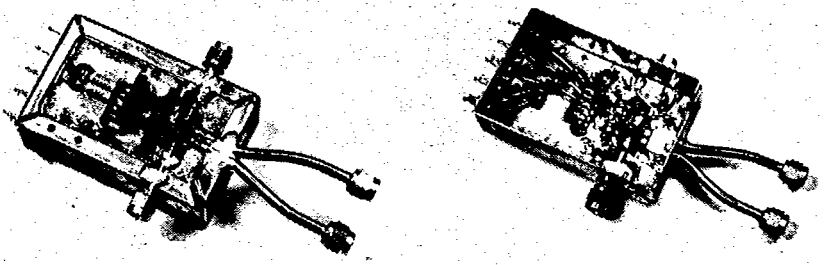


Fig. 15 - Printed-circuit board for the dynamic test circuit with components.



TOP VIEW
92CS-31652

BOTTOM VIEW
92CS-31653

Fig. 16 - Dynamic test circuit fixture.

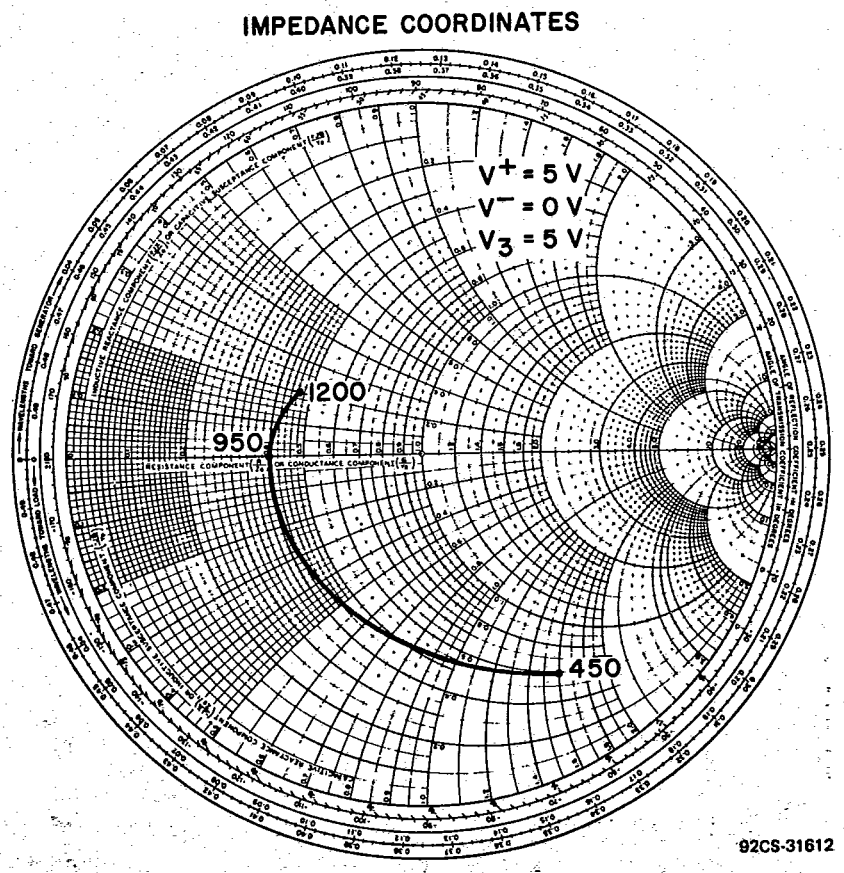


Fig. 17 - Impedance as a function of frequency.

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High-frequency construction and design techniques must be followed if the operation of the CA3179G test circuit is to be stable and if the results of repeated tests are to be consistent. The dynamic test circuit is shown in Fig. 3, and a photo of the test fixture that houses it is shown in Fig. 16. Listed below are some precautionary construction considerations for the circuit and test fixture.

1. Supply the ground plane with frequent ground connections.
2. Use 50-Ω coaxial cable for input connections
3. Use a "dead bug" type socket to minimize lead lengths and reduce series inductances
4. Use input pads that reduce impedance mismatch at the generator-test and meter-test input interfaces
5. Use leadless ceramic disc capacitors wherever possible
5. Provide capacitor by-passing near active terminals where ac grounds are required

Specific applications may require changes in the procedures listed above. The socket, for instance, can be eliminated by soldering the device directly to the p.c. board or by using individual board-mounted socket pins. Input and output interface connections and circuitry will also vary according to specific circuit requirements.

Partial Parts List for the Dynamic Test Circuit and Fixture:

4 Pasternac PE3493-6 SMA cable connectors and semi-rigid coaxial cable
1 Chassis
1 P.C. board
1 14-lead socket
2 1000-pF capacitors, Stettner Trush Inc. No. TEFIC-7
3 470-pF disc capacitors
3 1000-pF disc capacitors
2 33-pF feedthrough capacitors
3 1000-pF feedthrough capacitors
3 Ferrite beads, 0.375 x 0.187 x 0.250
2 Resistors, 390-Ω, ¼-W, 2%
1 Resistor, 56-Ω, 1/8-W, 5%
1 Resistor, 110-Ω, 1/8-W, 5%
1 Resistor, 9.1-Ω, 1/8-W, 5%
1 Resistor, 510-Ω, 1/8-W, 5%

Dimensions of Test Fixture

