3-Pin Microprocessor Reset Circuit

Features

- Precision monitoring of 3 V, 3.3 V and 5 V power supply voltages
- Fully specified over the temperature range of -40 to + 125 °C
- 140 ms minimum power-on reset pulse width:
  $\overline{\text{RESET}}$ output for V6309
  RESET output for V6319
- 16 µA supply current
- Garanteed $\overline{\text{RESET}}$/RESET valid to V_{DD} = 1 V
- Power supply transient immunity
- No external components needed
- 3-pin SOT23 package
- Fully compatible with MAX809/MAX810 and AMD809/AMD810

Description

The V6309 and V6319 are microprocessor supervisory circuits used to monitor the power supplies in µP and digital systems. They provide excellent circuit reliability and low cost by eliminating external components and adjustments when used with 5 V powered or 3 V powered circuits.

These circuits perform a single function: they assert a reset signal whenever the V_{DD} supply voltage declines below a preset threshold, keeping it asserted for at least 140 ms after V_{DD} has risen above the reset threshold. The only difference between the two devices is that the V6309 has an active-low $\overline{\text{RESET}}$ output (which is guaranteed to be in the correct state for V_{DD} down to 1 V), while the V6319 has an active-high RESET output. The reset comparator is designed to ignore fast transients on V_{DD}. Reset thresholds suitable for operation with a variety of supply voltages are available.

Low supply current makes the V6309/V6319 ideal for use in portable equipment. The V6309/V6319 come in a 3-pin SOT23 package

Applications

- Computers
- Controllers
- Intelligent instruments
- Critical µP and µC power monitoring
- Portable/battery-powered equipment

Typical Operating Configuration

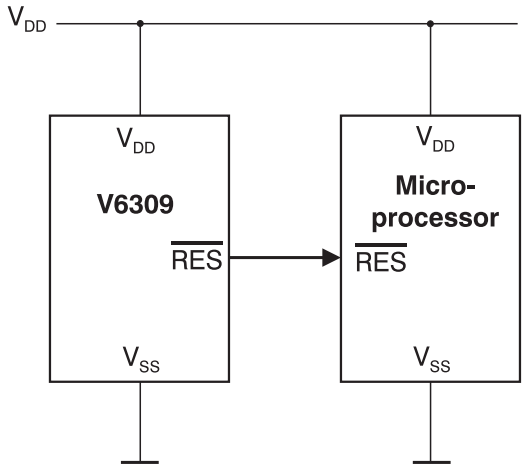


Fig. 1

Pin Assignment

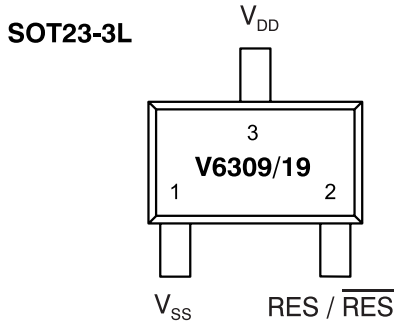


Fig. 2

Absolute Maximum Ratings

Parameter	Symbol	Conditions
Terminal voltage to V_{SS}	V_{DD}	-0.3 to 6.0 V
Min. voltage at Reset or $\overline{\text{Reset}}$	V_{min}	-0.3 V
Max. voltage at Reset or $\overline{\text{Reset}}$	V_{max}	V_{CC} + 0.3 V
Input current at V_{DD}	I_{min}	20 mA
Output current at Reset or $\overline{\text{Reset}}$	I_{max}	20 mA
Rate of rise at V_{DD}	t_R	100 Vµs
Continuous power dissipation at T_A = +70 °C for SOT-23 (>70 °C derate by 4 mW /°C)	P_{max}	320 mW
Operating temperature range	T_A	-40 to +125 °C
Storage temperature range	T_{ST}	-65 to +150 °C

Table 1

Stresses above these listed maximum ratings may cause permanent damage to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, anti-static precautions must be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the supply voltage range.

Electrical Characteristics

V_{DD} = full range, T_A = -40 to +125 °C unless otherwise specified, typical values are at T_A = +25 °C, V_{DD} = 5 V for versions L and M, V_{DD} = 3.3 V for versions T and S, V_{DD} = 3 V for version R.(Production testing done at T_A = +25°C and 85 °C, over temperature limits guaranteed by design only)

Parameter		Symbol	Test Conditions	Min.	Typ.	Max.	Units
V_{DD} range		V_{DD}	T_A = 0 to +70 °C	1.0		5.5	V
			T_A = -40 to +105 °C	1.2		5.5	V
			T_A = -40 to +125 °C	1.6		5.5	V
Supply current	versions L, M	I_{CC}	V_{DD}< 5.5 V		26	60	µA
	versions R,S,T		V_{DD} < 3.6 V		16	50	µA
Reset threshold[1]	version L	V_{TH}	T_A = +25 °C	4.56	4.63	4.70	V
			T_A = -40 to +125 °C	4.40		4.79	V
	version M		T_A = +25°C	4.31	4.38	4.45	V
			T_A = -40 to +125 °C	4.16		4.53	V
	version T		T_A = +25°C	3.04	3.08	3.11	V
			T_A = -40 to +125°C	2.92		3.17	V
	version S		T_A = +25 °C	2.89	2.93	2.96	V
			T_A = -40 to +125 °C	2.78		3.02	V
	version R		T_A = +25 °C	2.59	2.63	2.66	V
			T_A = -40 to +125°C	2.50		2.72	V
Reset threshold temp. coefficient					-200		ppm/°C
V_{DD} to reset delay[1]			V_{DD} = V_{TH} to (V_{TH} - 100 mV)		7		µs
Reset active timeout period			T_A = -40 to +125 °C	140	330	590	ms
$\overline{\text{Reset}}$ output voltage low for V6309	versions R,S,T	V_{OL}	V_{DD} > 1.0 V, I_{SINK} = 50 µA			0.3	V
			V_{DD} = V_{TH} min., I_{SINK} = 1.2 mA			0.3	V
	versions L, M		V_{DD} = V_{TH} min., I_{SINK} = 3.2 mA			0.4	V
$\overline{\text{Reset}}$ output voltage high for V6309							
	versions R,S,T	V_{OH}	V_{DD} > V_{TH} max., I_{SOURCE} = 500 µA	0.8 V_{DD}			V
	versions L, M		V_{DD} > V_{TH} max., I_{SOURCE} = 800 µA	V_{DD}-1.5 V			V
Reset output voltage low for V6319							
	versions R,S,T	V_{OL}	V_{DD} = V_{TH} max., I_{SINK} = 1.2 mA			0.3	V
	versions L, M		V_{DD} = V_{TH} max., I_{SINK} = 3.2 mA			0.4	V
Reset output voltage high for V6319		V_{OH}	1.8 V < V_{DD} < V_{TH} min., I_{SOURCE} = 150 µA	0.8 V_{DD}			V

[1] $\overline{\text{Reset}}$ output for V6309, Reset output for V6319

Table 2

Supply Current vs. Temperature
No load, V63xxR/S/T

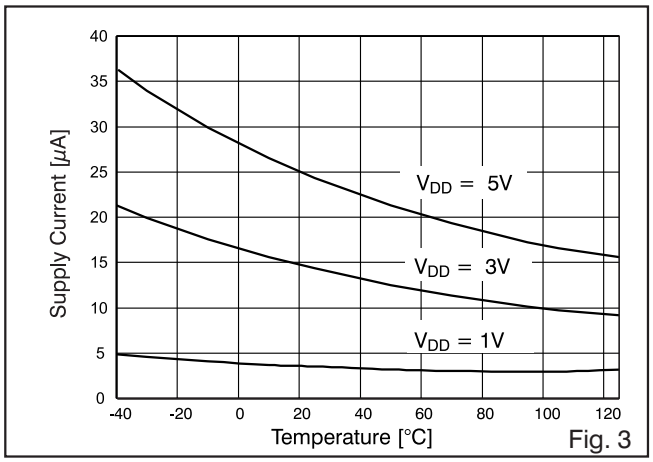


Fig. 3

Power-Down Reset Delay vs. Temperature
V63xxR/S/T

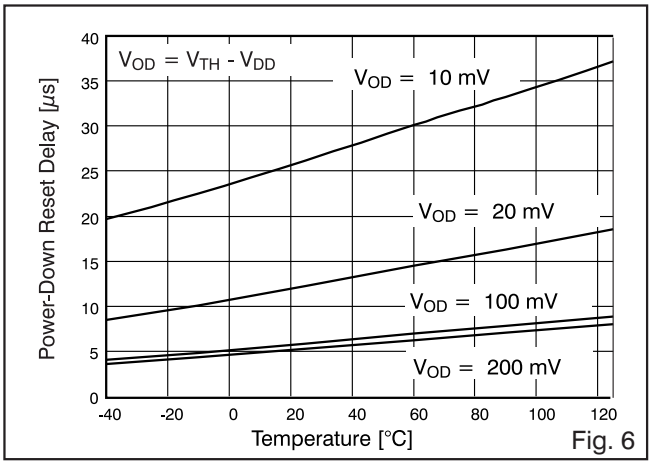


Fig. 6

Supply Current vs. Temperature
No load, V63xxL/M

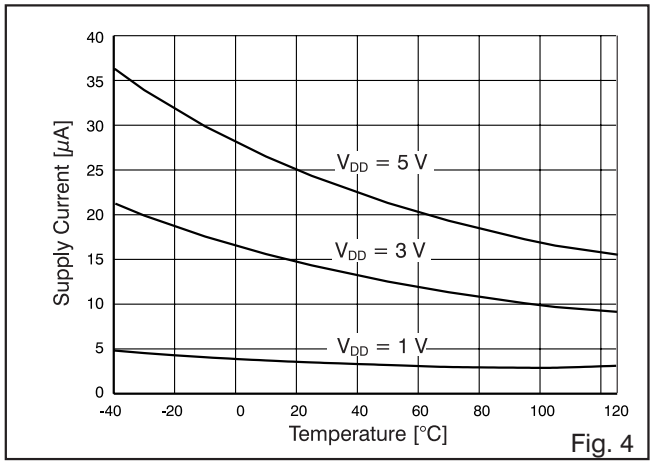


Fig. 4

Power-Down Reset Delay vs. Temperature
V63xxL/M

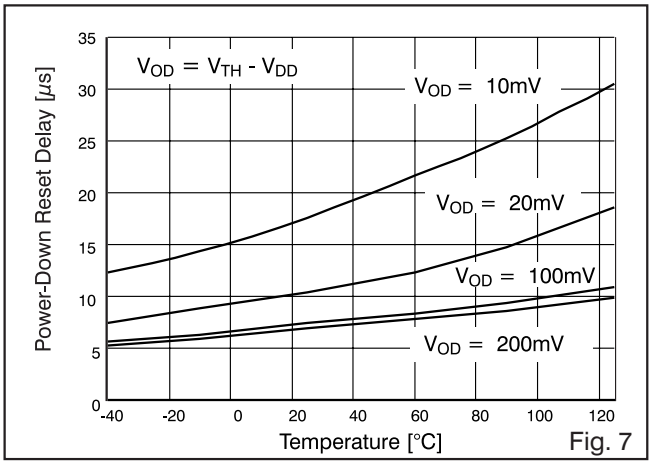


Fig. 7

Power-Up Reset Timeout vs. Temperature
All versions

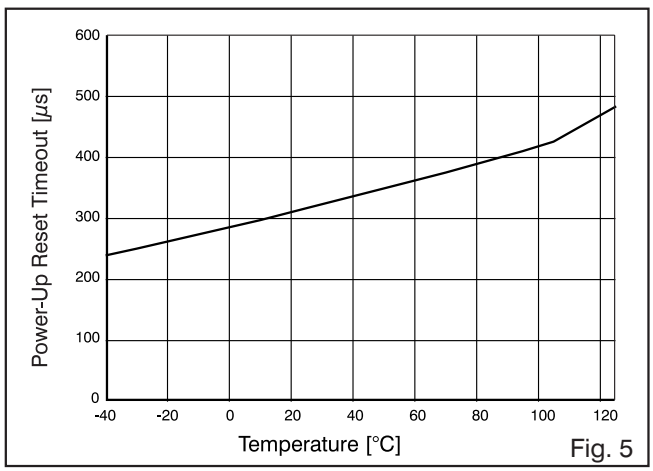


Fig. 5

Normalized Reset Threshold vs. Temperature
All versions

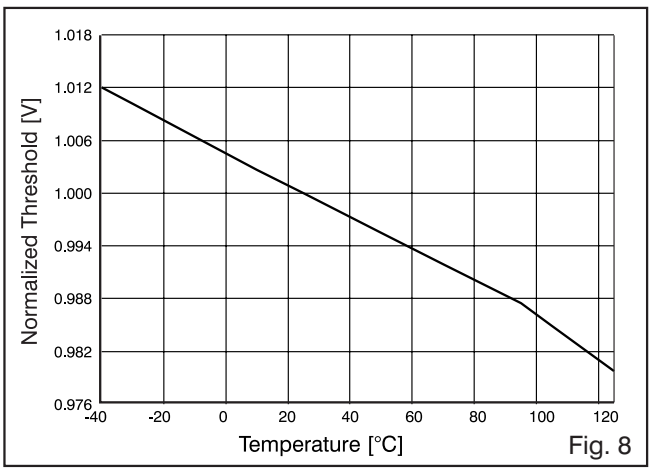


Fig. 8

Pin Description

Pin	Name	Function
1	V_{SS}	Ground
2	for V6309 $\overline{\text{RESET}}$	$\overline{\text{RESET}}$ Output remains low while V_{DD} is below the reset threshold and rises for 240 ms after V_{DD} above the reset threshold
2	for V6319 RESET	RESET Output remains high while V_{DD} is below the reset threshold and rises for 240 ms after V_{DD} above the reset
3	V_{DD}	Supply voltage (+5V, +3.3V or +3.0V)

Table 3

Application Information

Negative-Going V_{DD} Transients

In addition to issuing a reset to the microprocessor during power-up, power-down, and brownout conditions, the V6309/V6319 are relatively immune to short duration negative-going V_{DD} transients (glitches). Fig. 8 shows typical transient duration vs. Reset comparator overdrive, for which the V6309/V6319 do not generate a reset pulse. The graph was generated using a negative-going pulse applied to V_{DD}, starting 0.5 V above the actual reset threshold and ending below it by the magnitude indicated (reset comparator overdrive). The graph indicates the maximum pulse width a negative-going V_{DD} transient can have without causing a reset pulse. As the magnitude of the transient increases (goes farther below the reset threshold), the maximum allowable pulse width decreases. Typically, for the V6309L and V6319M, a V_{DD} transient that goes 100 mV below the reset threshold and lasts 20 µs or less will not cause a reset pulse. A 0.1 µF bypass capacitor mounted as close as possible to the V_{DD} pin provides additional transient immunity.

Max.Transient Duration without Causing a Reset Pulse versus Reset Comparator Overdrive

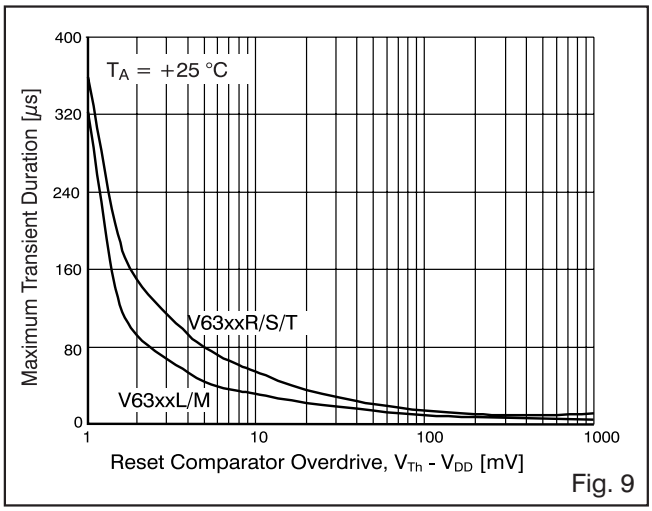


Fig. 9

Ensuring a Valid Reset Output down to V_{DD}= 0 V

When V_{DD} falls below 1 V, the V6309 $\overline{\text{RESET}}$ output no longer sinks current, it becomes an open circuit. Therefore, high-impedance CMOS logic inputs connected to $\overline{\text{RESET}}$ can drift to undetermined voltages. This presents no problem in most applications, since most µP and other circuitry is inoperative with V_{DD} below 1 V. However, in applications where $\overline{\text{RESET}}$ must be valid down to 0 V, adding a pull-down resistor to $\overline{\text{RESET}}$causes any stray leakage currents to flow to ground, holding $\overline{\text{RESET}}$ low (Fig.10). R1's value is not critical; 100 kΩ is large enough not to load $\overline{\text{RESET}}$ and small enough to pull $\overline{\text{RESET}}$ to ground. A 100 kΩ pull-up resistor to V_{DD} is also recommended for the V6319, if RESET is required to remain valid for V_{DD}<1 V.

RESET Valid for V_{DD} = Ground Circuit

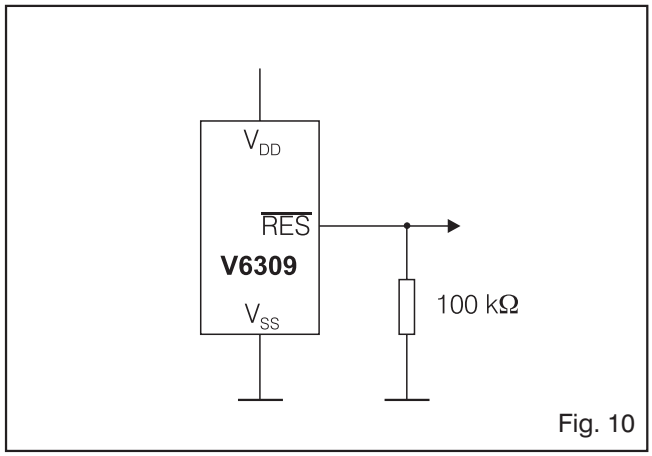


Fig. 10

Interfacing to µPs with Bidirectional Reset I/O

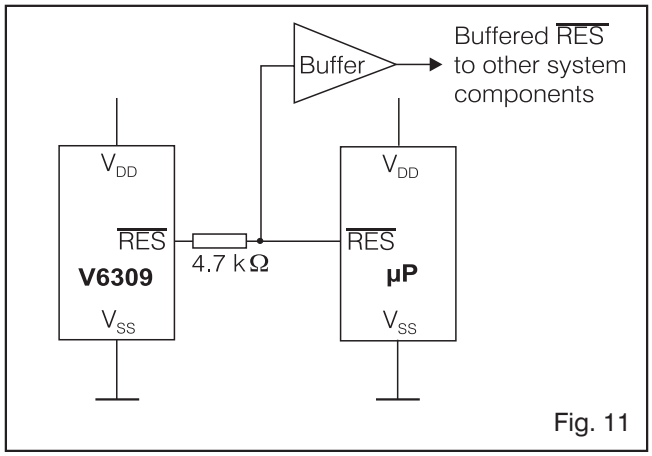


Fig. 11

Interfacing to µPs with Bidirectional Reset Pins

Microprocessors with bidirectional reset pins (such as the Motorola 68HC11 series) can connect to the V6309 reset output. If, for example, the V6309 $\overline{\text{RESET}}$ output is asserted high and the µP wants to pull it low, indeterminate logic levels may result. To correct this, connect a 4.7 kΩ resistor between the V6309 $\overline{\text{RESET}}$ output and the µP reset I/O (Fig. 11). Buffer the V6309 $\overline{\text{RESET}}$ output to other system components.

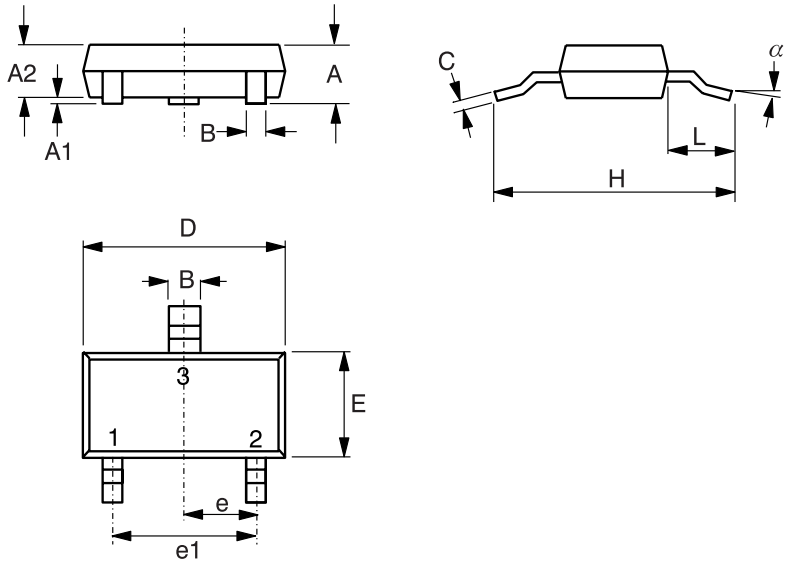
Benefits of Highly Accurate Reset Threshold

Most µP supervisor ICs have reset threshold voltages between 5% and 10% below the value of nominal supply voltages. This ensures a reset will not occur within 5% of the nominal supply, but will occur when the supply is 10% below nominal. When using ICs rated at only the nominal supply ±5%, this leaves a zone of uncertainty where the supply is between 5% and 10% low, and where the reset may or may not be asserted.

The V6309L/T and V6319L/T use highly accurate circuitry to ensure that reset is asserted close to the 5% limit, and long before the supply has declined to 10% below nominal.

Package and Ordering Information

Dimensions of SOT23-3L Package



Dimensions in mm

	Min.	Nom.	Max.
A	0.89	1.04	1.12
A1	0.013		0.10
A2	0.95	0.97	1.00
B	0.37		0.51
C	0.085	0.12	0.18
D	2.80	2.95	3.04
E	1.20	1.32	1.40
e		0.95	
e1	1.78	1.90	2.05
H	2.10	2.40	2.64
L	0.65		0.89
α	4°		6°

Ordering Information

When ordering, please always specify the complete Part Number. Please contact EM Microelectronic for availability.

Part Number	Threshold Voltage	Output Type	Package and Delivery Form	Top Marking [1] with 4 Characters	Top Marking [2] with 3 Characters
V6309RSP3B	2.63 V	Active low push-pull	SOT23-3L, Tape & Reel 3000 pces	AEAR	ER#
V6309SSP3B	2.93 V			AEAS	ES#
V6309TSP3B	3.08 V			AEAT	ET#
V6309MSP3B	4.38 V			AEAM	EM#
V6309LSP3B	4.63 V			AEAL	EL#
V6319RSP3B	2.63 V	Active high push-pull	SOT23-3L, Tape & Reel 3000 pces	AFAR	FR#
V6319SSP3B	2.93 V			AFAS	FS#
V6319TSP3B	3.08 V			AFAT	FT#
V6319MSP3B	4.38 V			AFAM	FM#
V6319LSP3B	4.63 V			AFAL	FL#

Table 4

[1] Top marking with 4 characters is standard from 2003.
[2] Top marking with 3 characters is kept as information since it was used until 2002. Where # refers to the lot number (EM internal reference only).

Traceability for small packages

Due to the limited space on the package surface, the bottom marking contains a limited number of characters that provide only partial information for lot traceability. Full information for complete traceability is however provided on the packing labels of the product at delivery from EM. It is highly recommended that the customer insures full lot traceability of EM product in his final product.