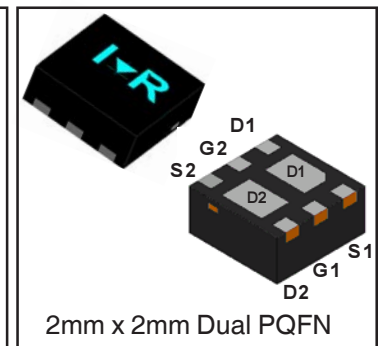
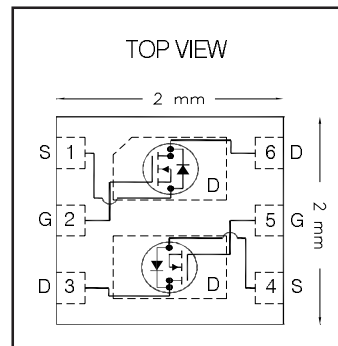


$V_{DS}$	<b>30</b>	<b>V</b>
$V_{GS}$	<b>±12</b>	<b>V</b>
$R_{DS(on) max}$ (@ $V_{GS} = 4.5V$ )	<b>63</b>	<b>mΩ</b>
$R_{DS(on) max}$ (@ $V_{GS} = 2.5V$ )	<b>82</b>	<b>mΩ</b>
$I_D$ (@ $T_{c(Bottom)} = 25°C$ )	<b>3.4</b> Ⓣ	<b>A</b>



## Applications

- Charge and discharge switch for battery application
- Load/System Switch

## Features and Benefits

### Features

Low $R_{DS(on)}$ ( $\leq 63m\Omega$ )
Low Thermal Resistance to PCB ( $\leq 19°C/W$ )
Low Profile ( $\leq 1.0mm$ )
Industry-Standard Pinout
Compatible with Existing Surface Mount Techniques
RoHS Compliant Containing no Lead, no Bromide and no Halogen

results in  
⇒

### Resulting Benefits

Lower Conduction Losses
Enable better thermal dissipation
Increased Power Density
Multi-Vendor Compatibility
Easier Manufacturing
Environmentally Friendlier

Orderable part number	Package Type	Standard Pack		Note
		Form	Quantity	
IRLHS6376TRPBF	PQFN Dual 2mm x 2mm	Tape and Reel	4000	
IRLHS6376TR2PBF	PQFN Dual 2mm x 2mm	Tape and Reel	400	

## Absolute Maximum Ratings

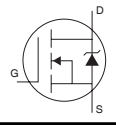
	Parameter	Max.	Units
$V_{DS}$	Drain-to-Source Voltage	30	V
$V_{GS}$	Gate-to-Source Voltage	±12	
$I_D @ T_A = 25°C$	Continuous Drain Current, $V_{GS} @ 4.5V$	3.6Ⓣ	A
$I_D @ T_A = 70°C$	Continuous Drain Current, $V_{GS} @ 4.5V$	2.9	
$I_D @ T_{C(Bottom)} = 25°C$	Continuous Drain Current, $V_{GS} @ 4.5V$	7.6Ⓣ	
$I_D @ T_{C(Bottom)} = 100°C$	Continuous Drain Current, $V_{GS} @ 4.5V$	4.9Ⓣ	
$I_D @ T_{C(Bottom)} = 25°C$	Continuous Drain Current, $V_{GS} @ 4.5V$ (Package Limited)	3.4Ⓣ	
$I_{DM}$	Pulsed Drain Current ①	30	
$P_D @ T_A = 25°C$	Power Dissipation ④	1.5	W
$P_D @ T_{C(Bottom)} = 25°C$	Power Dissipation ④	6.6	
	Linear Derating Factor ④	0.012	W/°C
$T_J$ $T_{STG}$	Operating Junction and Storage Temperature Range	-55 to + 150	°C

Notes ① through ④ are on page 2

### Static @ T<sub>J</sub> = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
B <sub>V</sub> DSS	Drain-to-Source Breakdown Voltage	30	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
ΔB <sub>V</sub> DSS/ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	—	0.023	—	V/°C	Reference to 25°C, I <sub>D</sub> = 1mA
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	48	63	mΩ	V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 3.4A ③②
		—	61	82		V <sub>GS</sub> = 2.5V, I <sub>D</sub> = 3.4A ③②
V <sub>GS(th)</sub>	Gate Threshold Voltage	0.5	0.8	1.1	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 10μA
ΔV <sub>GS(th)</sub>	Gate Threshold Voltage Coefficient	—	-3.6	—	mV/°C	
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	1.0	μA	V <sub>DS</sub> = 24V, V <sub>GS</sub> = 0V
		—	—	150		V <sub>DS</sub> = 24V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	100	nA	V <sub>GS</sub> = 12V
	Gate-to-Source Reverse Leakage	—	—	-100		V <sub>GS</sub> = -12V
g <sub>fs</sub>	Forward Transconductance	8.8	—	—	S	V <sub>DS</sub> = 10V, I <sub>D</sub> = 3.4A②
Q <sub>g</sub>	Total Gate Charge ⑥	—	2.8	—	nC	V <sub>DS</sub> = 15V
Q <sub>gs</sub>	Gate-to-Source Charge ⑥	—	0.13	—		V <sub>GS</sub> = 4.5V
Q <sub>gd</sub>	Gate-to-Drain Charge ⑥	—	1.1	—		I <sub>D</sub> = 3.4A② (See Fig.17 & 18)
R <sub>G</sub>	Gate Resistance	—	4.6	—	Ω	
t <sub>d(on)</sub>	Turn-On Delay Time	—	4.4	—	ns	V <sub>DD</sub> = 10V, V <sub>GS</sub> = 4.5V
t <sub>r</sub>	Rise Time	—	11	—		I <sub>D</sub> = 3.4A②
t <sub>d(off)</sub>	Turn-Off Delay Time	—	11	—		R <sub>G</sub> = 1.8Ω
t <sub>f</sub>	Fall Time	—	9.4	—		See Fig.15
C <sub>iss</sub>	Input Capacitance	—	270	—	pF	V <sub>GS</sub> = 0V
C <sub>oss</sub>	Output Capacitance	—	32	—		V <sub>DS</sub> = 25V
C <sub>rss</sub>	Reverse Transfer Capacitance	—	20	—		f = 1.0MHz

### Diode Characteristics

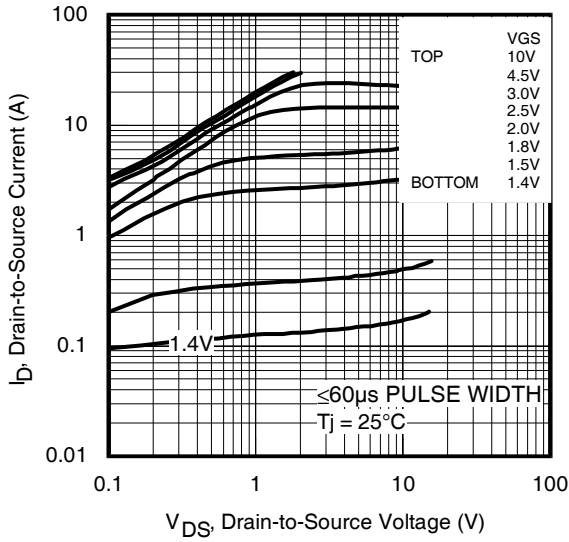
	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	7.6⑥	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①	—	—	30		
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.2	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 3.4A②, V <sub>GS</sub> = 0V ③
t <sub>rr</sub>	Reverse Recovery Time	—	8.0	12	ns	T <sub>J</sub> = 25°C, I <sub>F</sub> = 3.4A②, V <sub>DD</sub> = 15V
Q <sub>rr</sub>	Reverse Recovery Charge	—	5.9	8.9	nC	di/dt = 260A/μs ③
t <sub>on</sub>	Forward Turn-On Time	Time is dominated by parasitic Inductance				

### Thermal Resistance

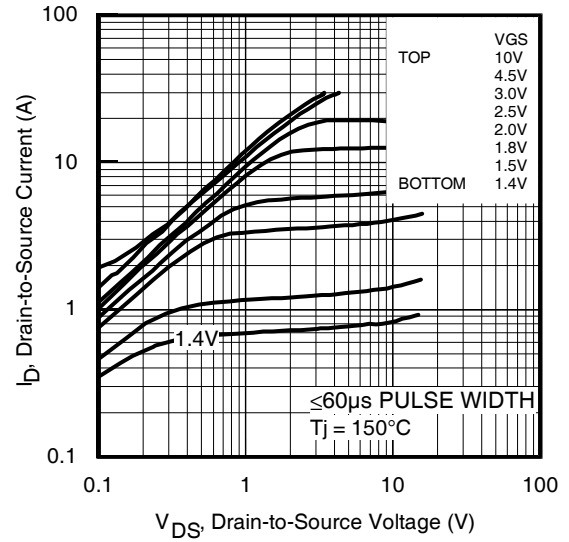
	Parameter	Typ.	Max.	Units
R <sub>θJC</sub> (Bottom)	Junction-to-Case ⑤	—	19	°C/W
R <sub>θJC</sub> (Top)	Junction-to-Case ⑤	—	175	
R <sub>θJA</sub>	Junction-to-Ambient ④	—	86	
R <sub>θJA</sub> (<10s)	Junction-to-Ambient ④	—	69	

#### Notes:

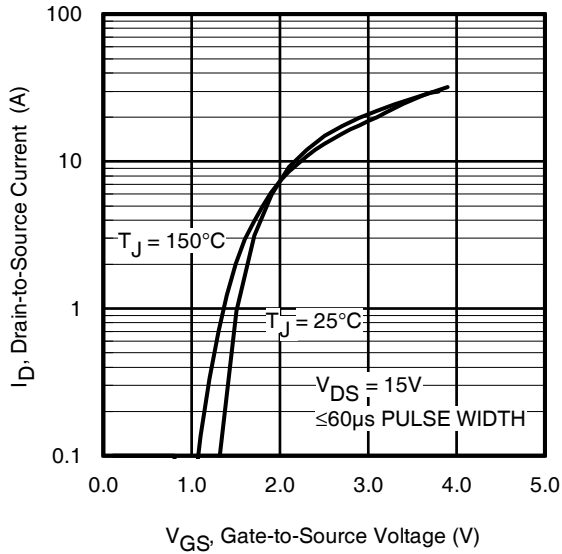
- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Current limited by package.
- ③ Pulse width ≤ 400μs; duty cycle ≤ 2%.
- ④ When mounted on 1 inch square copper board.
- ⑤ R<sub>θ</sub> is measured at T<sub>J</sub> of approximately 90°C.
- ⑥ For DESIGN AID ONLY, not subject to production testing.



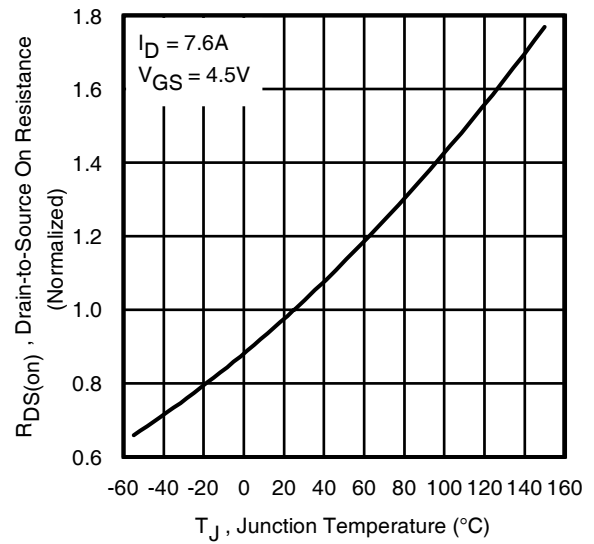
**Fig 1.** Typical Output Characteristics



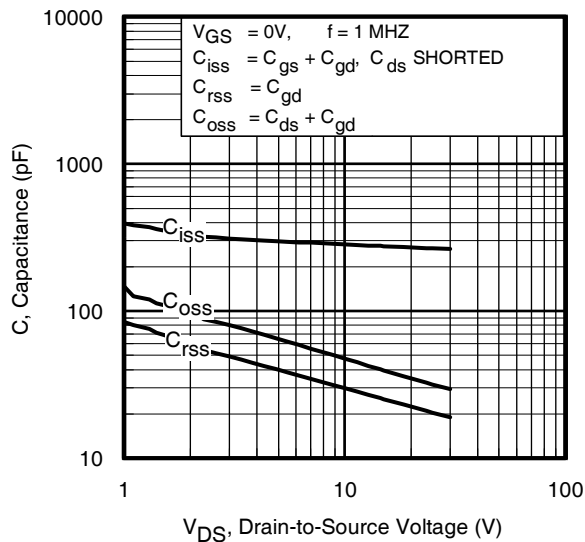
**Fig 2.** Typical Output Characteristics



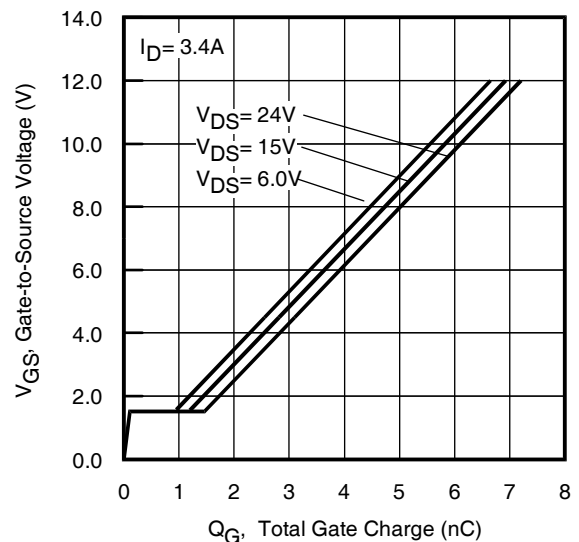
**Fig 3.** Typical Transfer Characteristics



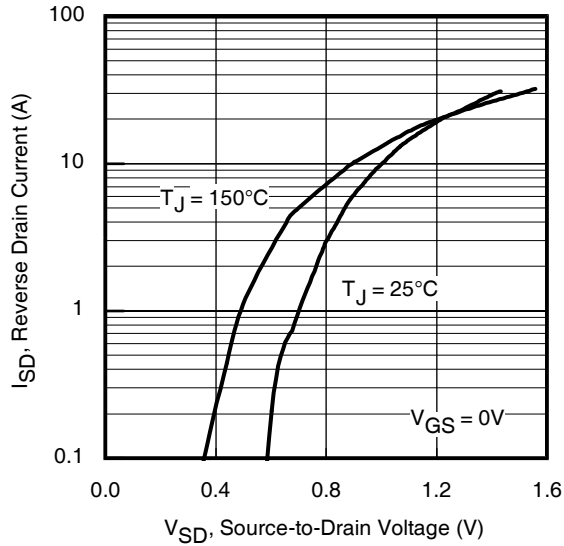
**Fig 4.** Normalized On-Resistance vs. Temperature



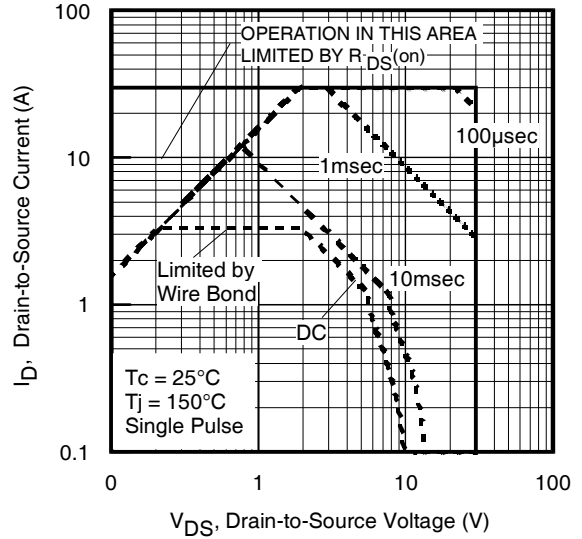
**Fig 5.** Typical Capacitance vs. Drain-to-Source Voltage



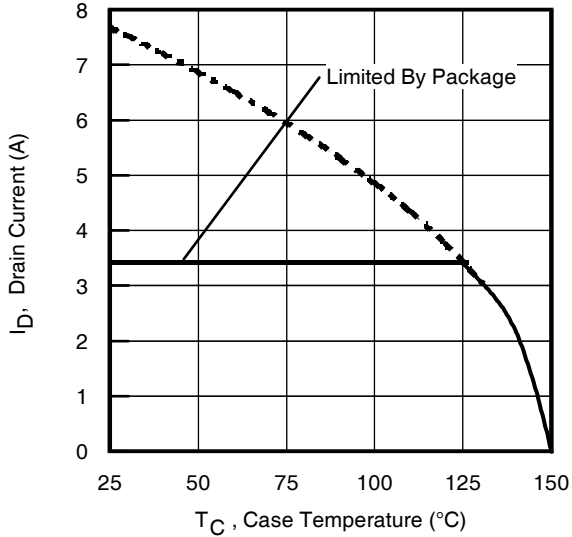
**Fig 6.** Typical Gate Charge vs. Gate-to-Source Voltage



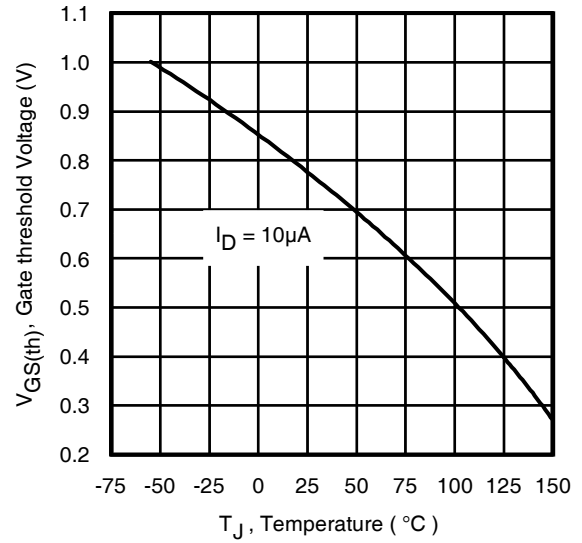
**Fig 7.** Typical Source-Drain Diode Forward Voltage



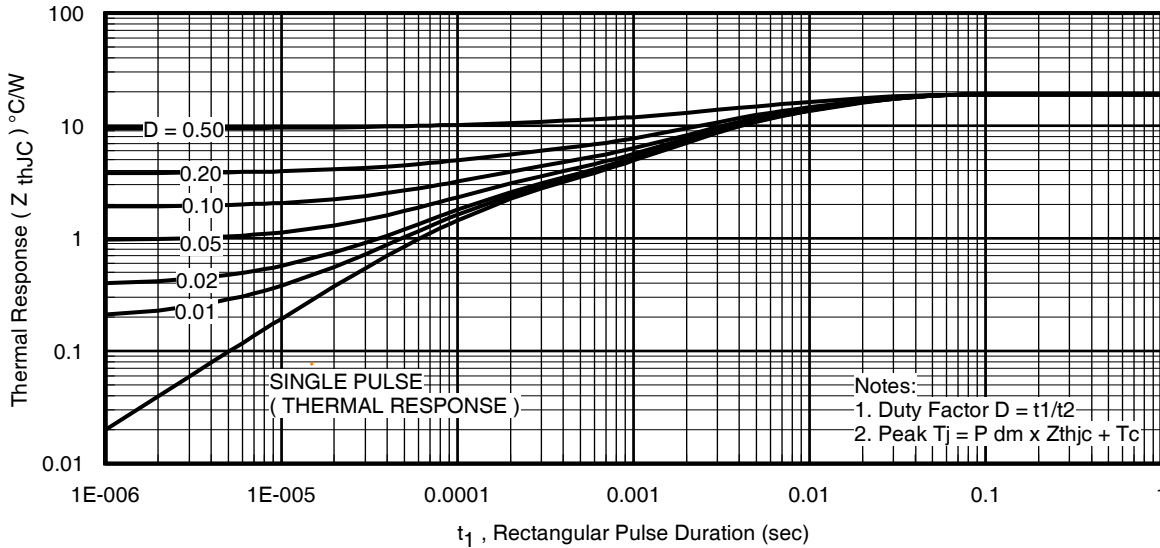
**Fig 8.** Maximum Safe Operating Area



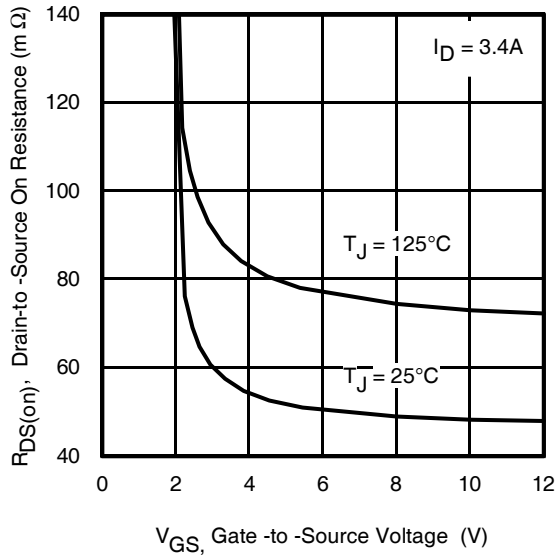
**Fig 9.** Maximum Drain Current vs. Case (Bottom) Temperature



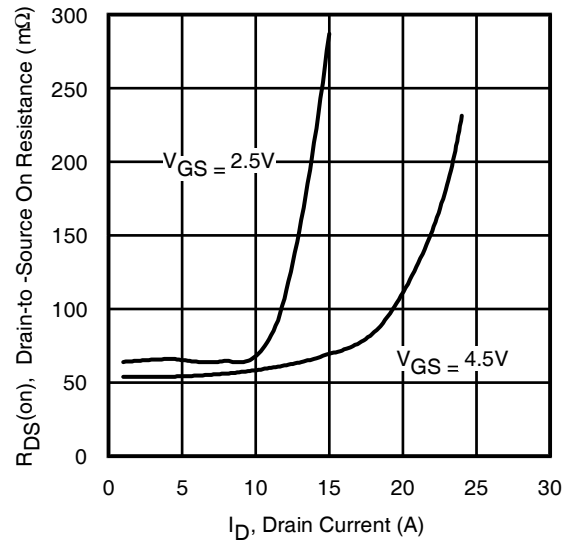
**Fig 10.** Threshold Voltage vs. Temperature



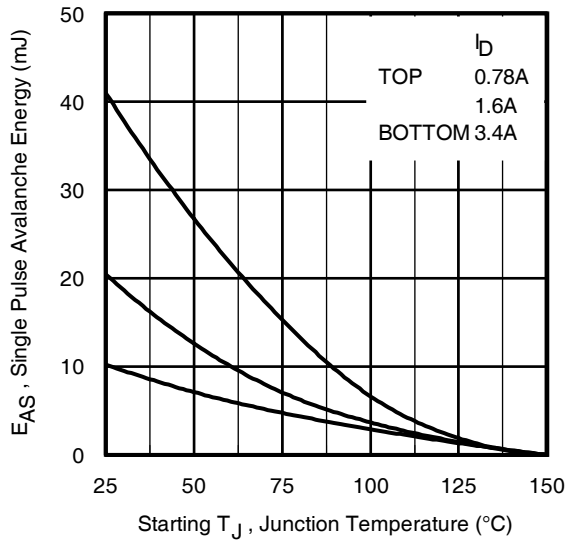
**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case (Bottom)



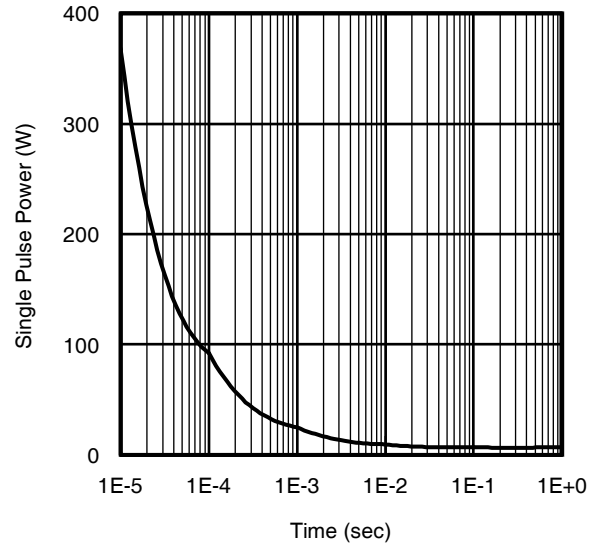
**Fig 12.** On-Resistance vs. Gate Voltage



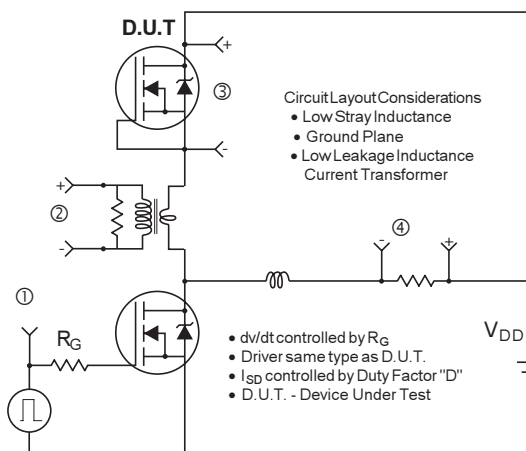
**Fig 13.** Typical On-Resistance vs. Drain Current



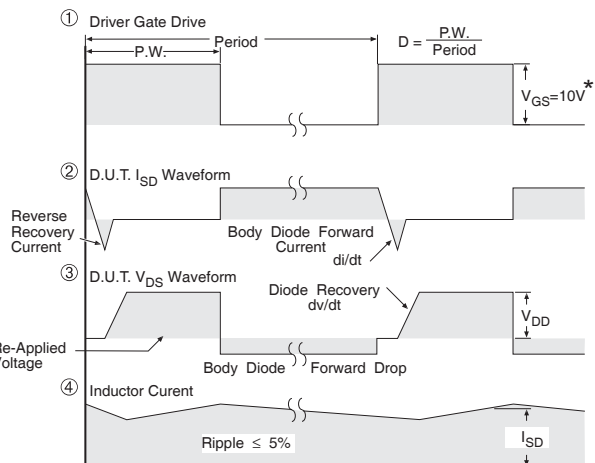
**Fig 14.** Maximum Avalanche Energy vs. Drain Current



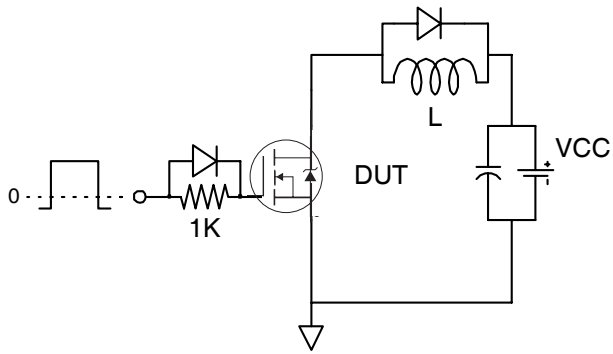
**Fig 15.** Typical Power vs. Time



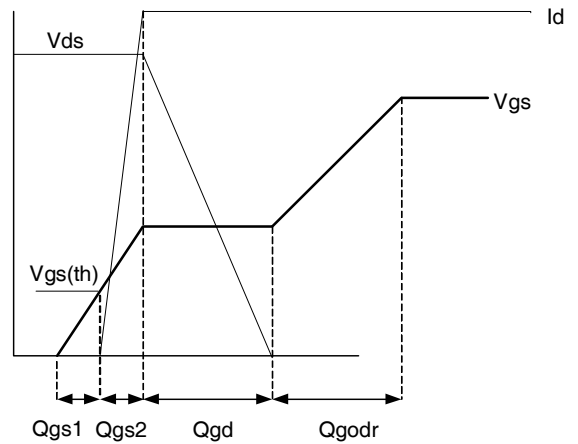
**Fig 16.** Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETS



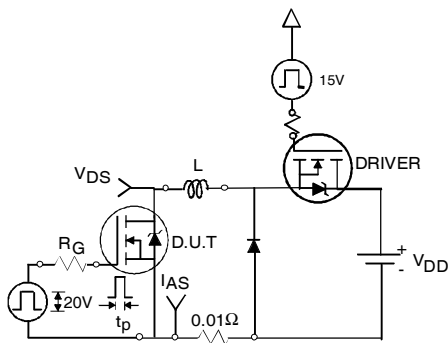
\*  $V_{GS} = 5V$  for Logic Level Devices



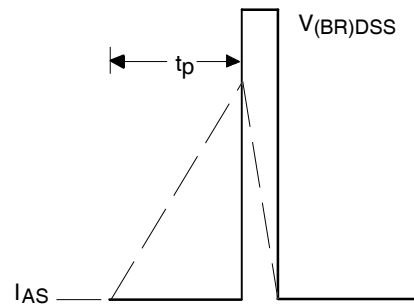
**Fig 17a.** Gate Charge Test Circuit



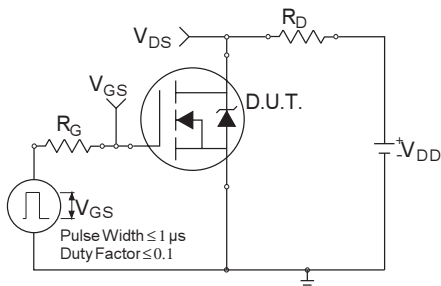
**Fig 17b.** Gate Charge Waveform



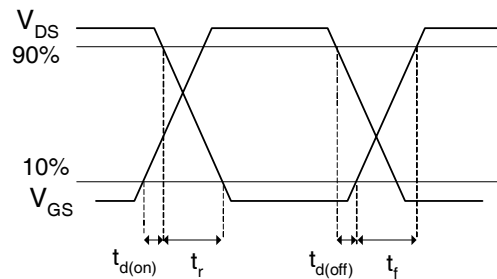
**Fig 18a.** Unclamped Inductive Test Circuit



**Fig 18b.** Unclamped Inductive Waveforms

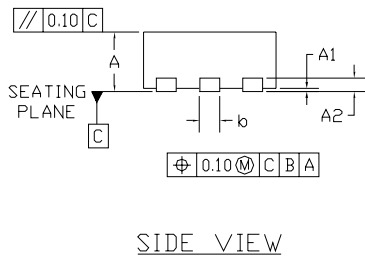
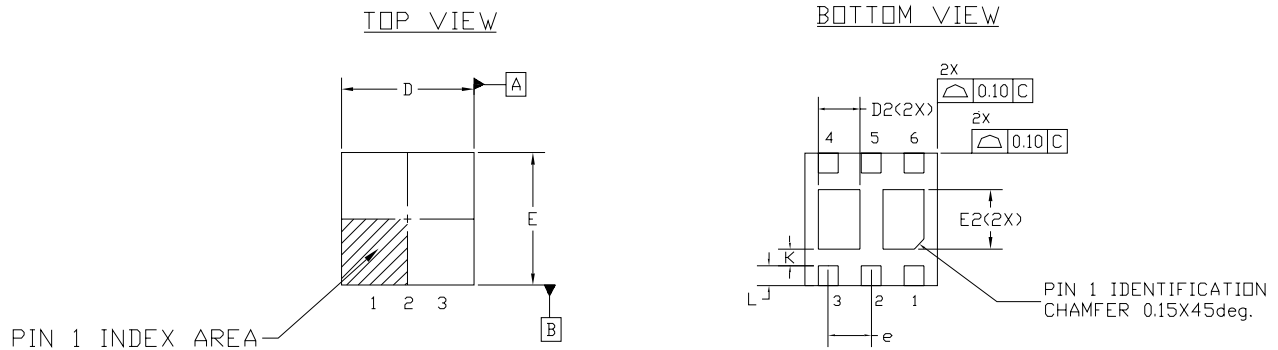


**Fig 19a.** Switching Time Test Circuit



**Fig 19b.** Switching Time Waveforms

## PQFN Dual 2x2 Outline Package Details



SYMBOL	COMMON					
	DIMENSIONS MILLIMETER			DIMENSIONS INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.90	1.00	0.032	0.036	0.040
A1	0.00	0.02	0.05	0.000	0.001	0.002
A2	0.203 REF			0.008 REF		
b	0.25	0.30	0.35	0.010	0.012	0.014
D	1.90	2.00	2.10	0.075	0.079	0.083
D2	0.575	0.625	0.675	0.023	0.025	0.027
E	1.90	2.00	2.10	0.075	0.079	0.083
E2	0.85	0.90	0.95	0.034	0.036	0.038
e	0.65 BSC			0.026 BSC		
L	0.25	0.30	0.35	0.010	0.012	0.014
K	0.25	-	-	0.010	-	-

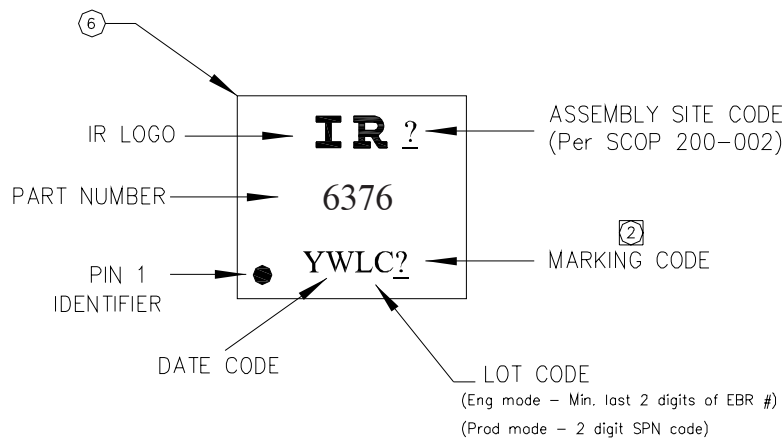
NOTES :

1. DIMENSION AND TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. CONTROLLING DIMENSIONS : MILLIMETER. CONVERTED INCH DIMENSION ARE NOT NECESSARILY EXACT.

For footprint and stencil design recommendations, please refer to application note AN-1154 at <http://www.irf.com/technical-info/appnotes/an-1154.pdf>

## PQFN Dual 2x2 Outline Part Marking

TOP MARKING (LASER)



Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>  
www.irf.com

## PQFN Dual 2x2 Outline Tape and Reel

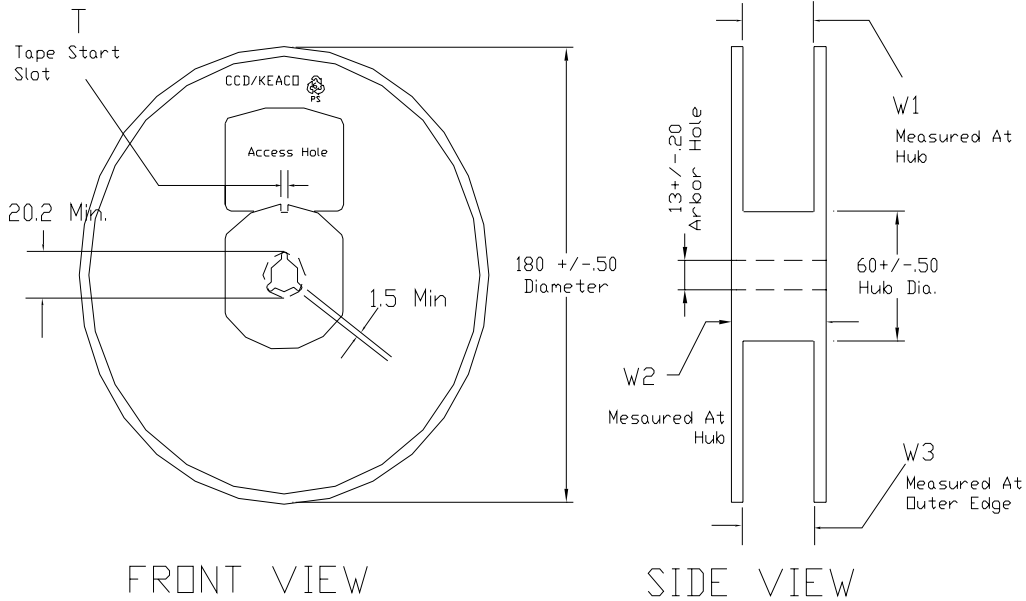
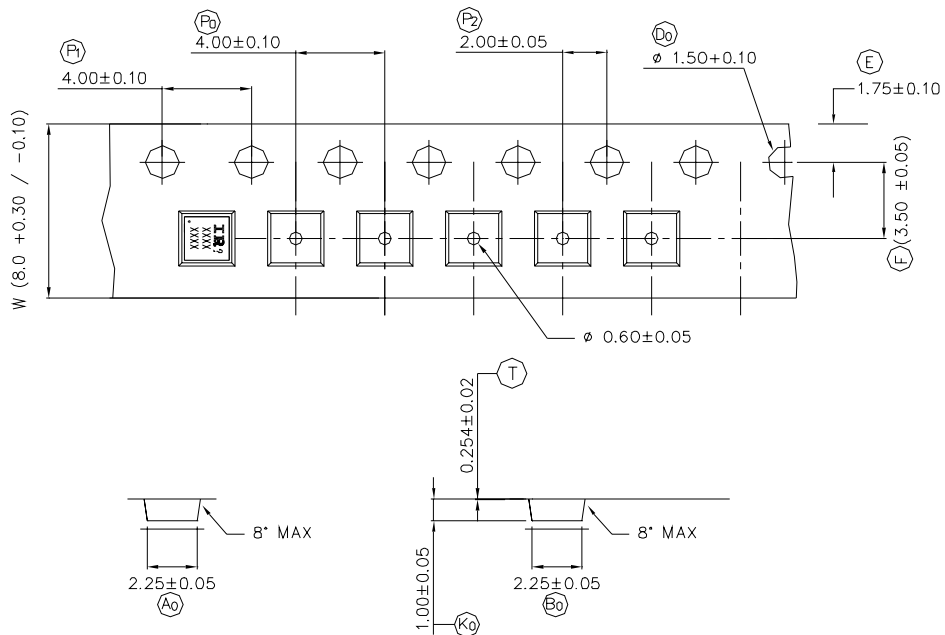


TABLE 1: REEL DETAILS

TAPE WIDTH	T	W1	W2	W3	PART NO
8 MM	3 ± 0.50	8.4 <sup>+1.5</sup> <sub>-0.0</sub>	14.4 Max	7.90 Min 10.9 Max	91586-1
12 MM	5 ± 0.50	12.4 <sup>+2.0</sup> <sub>-0.0</sub>	18.4 Max	11.9 Min 15.4 Max	91586-2

Note: Surface resistivity is  $\geq 1 \times 10^5$  but  $< 1 \times 10^{12}$  ohm/sq.



NOTE: The Surface Resistivity is  $10^4 - 10^8$  OHM/SQ



**Qualification information<sup>†</sup>**

Qualification level	Consumer <sup>††</sup> (per JEDEC JESD47F <sup>†††</sup> guidelines )	
Moisture Sensitivity Level	PQFN Dual 2mm x 2mm	MSL1 (per JEDEC J-STD-020D <sup>†††</sup> )
RoHS compliant	Yes	

† Qualification standards can be found at International Rectifier's web site  
<http://www.irf.com/product-info/reliability>

†† Higher qualification ratings may be available should the user have such requirements.  
 Please contact your International Rectifier sales representative for further information:  
<http://www.irf.com/whoto-call/salesrep/>

††† Applicable version of JEDEC standard at the time of product release.

Data and specifications subject to change without notice.

International  
**IR** Rectifier

**IR WORLD HEADQUARTERS:** 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105  
 TAC Fax: (310) 252-7903

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